MF012K6VPX LDMOS TRANSISTOR

Document Number: MF012K6VPX
Preliminary Datasheet V1.0

2600W, 50V High Power LDMOS FETs

MF012K6VPX

Description

The MF012K6VPX is a 50V 2600W capable, high performance, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 225MHz.It can be used for both CW and pulse application.It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, HF communication, VHF TV and Aerospace applications.

Please notice that due to internal configuration of both input and output leads, dual path of this device must be configured as in-phase combination, NOT 180dgree Balun or 90 degree hybrid combination.

- Typical Performance (On Innogration in-phase combiner narrowband fixture with device soldered):

Freq(MHz)	Voltage(V)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)	$2^{nd}/3^{rd}$ (dBc)	Remark
13.56	50	Pulse	45	3100	20	75	/	High power tuning
13.56	36	CW	41	1650	21	78	-49/-60	
13.56	50	CW	42	2500	22	81	-47/-63	High Eff tuning

Features

- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	165	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+60	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 2600W CW, 50 Vdc, I_{DQ} = 250 mA	$R_{\theta JC}$	0.10	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.015	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

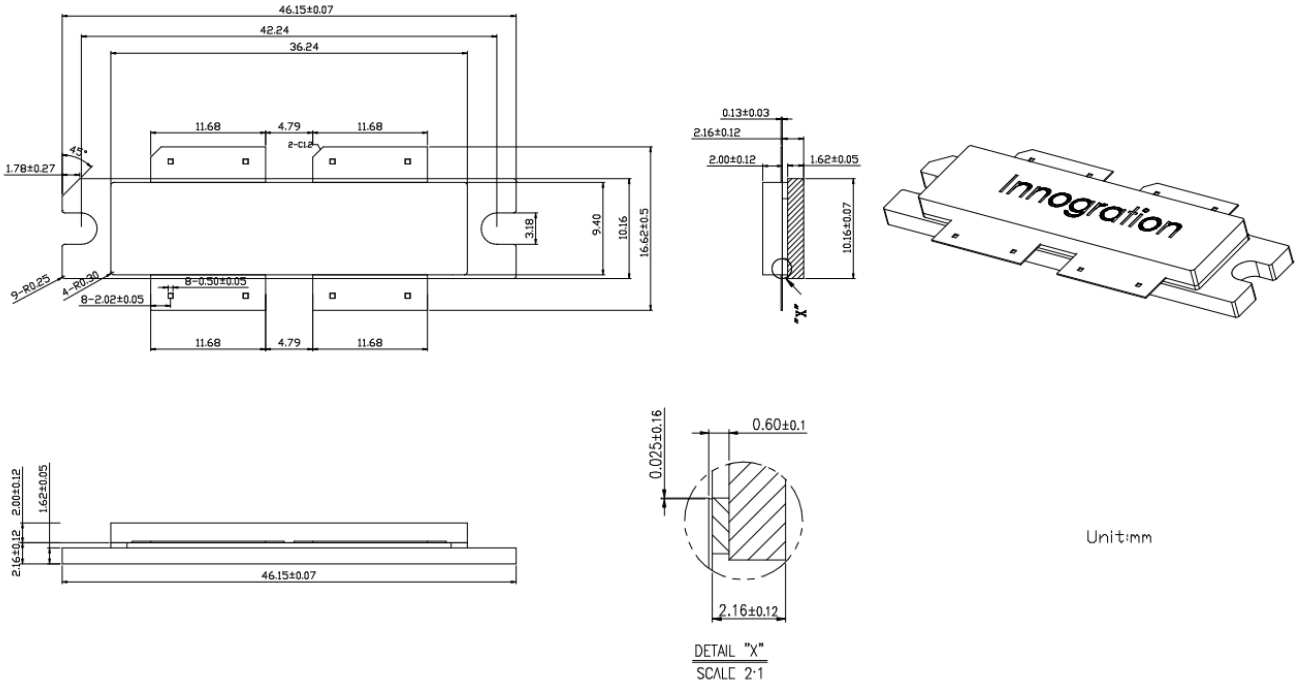
Characteristic	Symbol	Min	Typ	Max	Unit

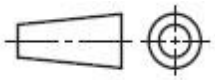
DC Characteristics

Drain-Source Voltage V_{GS}=0, I_{DS}=20.0mA	$V_{(BR)DSS}$		165		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	3	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 250 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.25	——	V

Package Outline

Flanged ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-O4E					**5/6/2024**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/3/5	Rev 1.0	Preliminary Datasheet

Application data based on SYX-26-13

Disclaimers