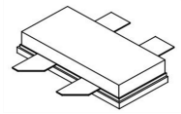


MK0918GS LDMOS TRANSISTOR

Document Number: MK0918GS
Product Datasheet V1.0

180W, P band High Power RF LDMOS FETs

MK0918GS



Description

The MK0918GS is a 180-watt, both input and output matched, high ruggedness, push pull LDMOS FETs, designed for P band and UHF application within 0.5 to 1.2GHz.

- Typical RF Performance under CW (On Innogration fixture with device soldered):

MK0918GS ^{V0} VGS=2.40V VDS=28V IDQ=200mA CW								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff (%)	2nd (dBc)	3rd (dBc)
500	52.75	188.4	11.26	40.50	12.25	59.75	-21.40	-27.50
600	53.02	200.4	11.30	39.00	14.02	63.35	-18.40	-57.30
700	52.14	163.7	9.14	41.10	11.04	63.96	-25.30	-48.50
800	52.34	171.4	9.98	41.00	11.34	61.34	-44.70	-58.00
900	52.83	191.9	11.61	41.10	11.73	59.02	-67.00	-51.70
1000	52.96	197.7	12.10	41.70	11.26	58.35	-51.40	-41.00
1100	53.06	202.3	11.32	41.70	11.36	63.83	-51.50	-44.00
1200	51.90	154.9	9.11	41.40	10.50	60.72	-51.70	-55.80

Features

- High Efficiency and Linear Gain Operations
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Pb-free, RoHS-compliant

Suitable Applications

- P band pulse or CW amplifier
- UHF band pulsed amplifier
- Test measurement applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _{case} =25°C; CW	R _{θJC}	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 65V, V _{GS} = 0 V)	I _{loss}			100	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{loss}			1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{loss}			1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 450 μA)	V _{GS(th)}		1.9		V
Gate Quiescent Voltage (V _{DD} = 28 V, I _D = 1.2A, Measured in Functional Test)	V _{GS(Q)}		2.7		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 1000 MHz

VSWR 5:1 at 180W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 2. Test Circuit Component Layout

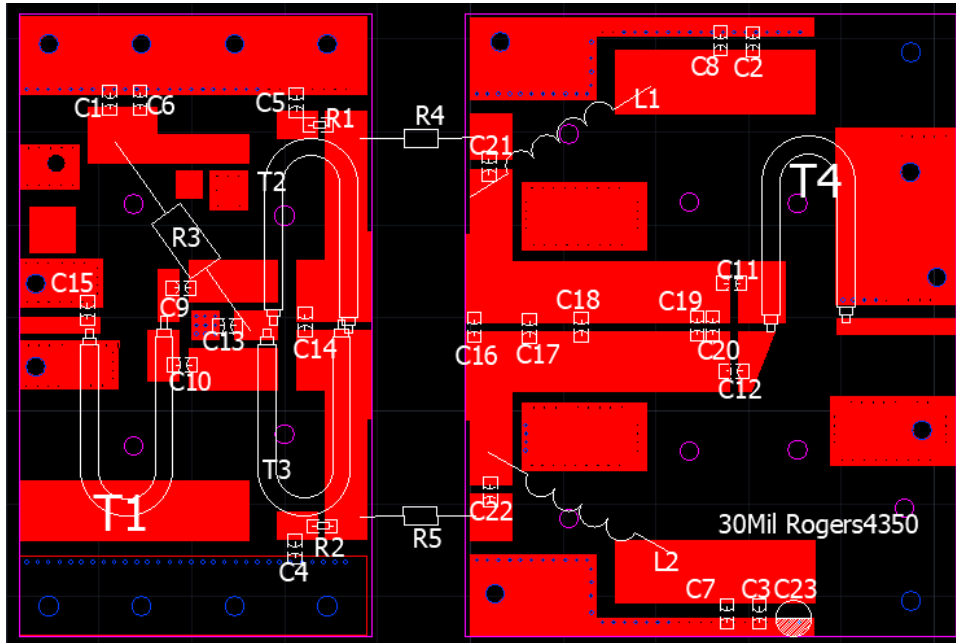


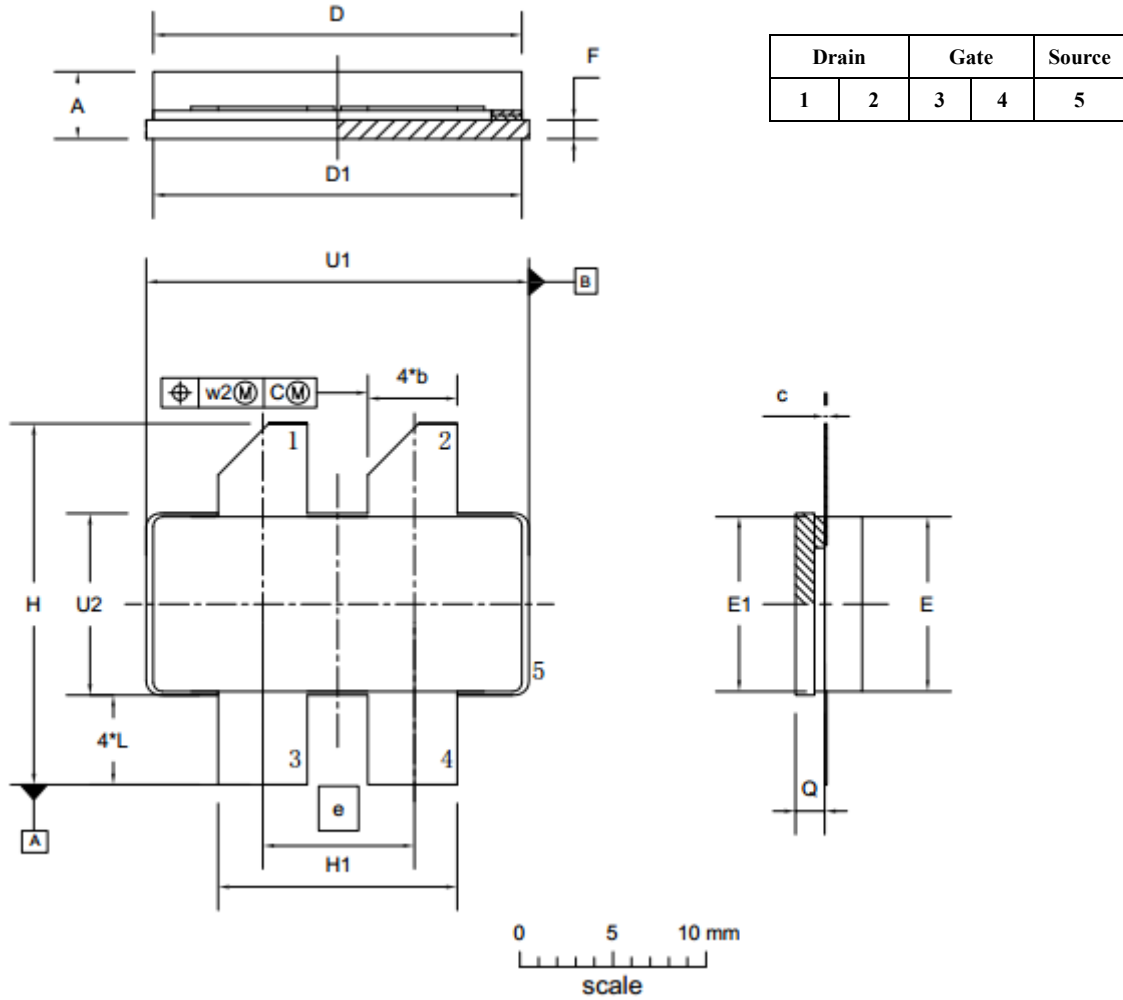
Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1~C5,C13	10uF/200V-1210	Ceramic multilayer capacitor
C6~C8	470pF	
C9,C10	27pF	
C11,C12	33pF	
C14	1.8pF	
C15	0.5pF	
C16	9.1pF	
C17	1pF	
C18	1.2pF	
C19	0.8pF	
C20	3.9pF	
C21,C22	1000pF	
R1,R2	10 Ω /2512	Chip Resistor
R3	300 Ω	color ring resistor
R4,R5	470 Ω	color ring resistor
T1	50 ohm-30mm	RFSFBU-086-50
T2,T3	16.7 ohm-30mm	SFF-16.7-1.5
T4	35ohm-45mm	SFF-35-3
L1,L2	1.5mm wire , 5mm inner diameter, 1Turns	DIY

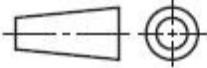
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Earless Flanged Ceramic Package; 4 leads



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/4/15	Rev 1.0	Product Datasheet

Application data based on TC-26-12

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