80W, 50V ,2.2GHz High Power RF LDMOS FETs

ITGV20080T2C

Description

The ITGV20080T2C is a 60-watt, LDMOS FET, designed for mulitiple applications up to 2.2GHz. It can be used in Class AB/B and Class C configuration, supporting both CW and pulsed signal

- Typical Performance at different bands (On Innogration fixture with device soldered):

Vds= 50V, Vgs=3.2V,Idq=100mA						
Freq(MHz)	**Test signal**	**P-1(dBm)**	**P-1Gain(dB)**	**P-3(dBm)**	**P-3(W)**	**Eff (%)**
1400	**Pulsed/CW**	**48.69**	**18.91**	**49.47**	**88**	**60**
1800-1900 *	**Pulsed**	**48.47**	**15.86**	**49.34**	**85**	**55**
2100-2200*	**Pulsed**	**48.02**	**16.7**	**48.90**	**78**	**50**

***At back off， it can meet -50dBc ACPR at 37dBm as high linear driver for 50V GaN Doherty**

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, Pout=60W 915MHz	$R_{\theta JC}$	0.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	106	——	——	V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current	I_{GSS}	——	——	1	μA

(V_{GS} = 6 V, V_{DS} = 0 V)					
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$	——	3	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} =100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.3		V

Functional Tests (On Innogration Test Fixture, 50 ohm system) : V_{DD} =50Vdc, I_{DQ} =50 mA, f = 1.4GHz, Pin=31dBm CW Signal Measurements.

Power Gain	Gp	——	17	——	dB
Drain Efficiency @ P_{OUT}	η_D	——	60	——	%
Output Power	P_{out}	——	8	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 50 mA, f = 2000 MHz

VSWR 10:1 at 80W Output Power at all Phase Angles, pulsed CW, 100us, 10%	No Device Degradation

2100-2200MHz
Reference Circuit of Test Fixture Assembly Diagram

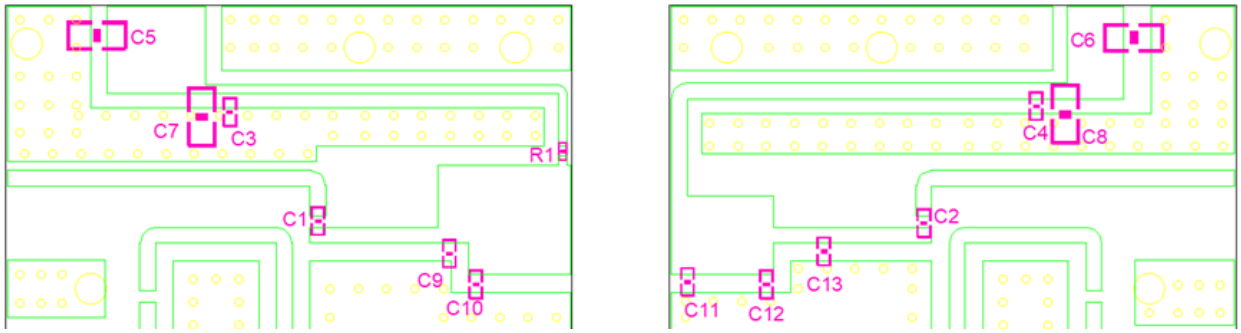


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Part	Quantity	Description	Part Number	Manufacture
C1,C11	2	3.9pFHigh Q Capacitor	251SHS3R9BSE	TEMEX
C2,C3,C4	3	20pFHigh Q Capacitor	251SHS200BSE	TEMEX
C9	1	0.4pFHigh Q Capacitor	251SHS0R4BSE	TEMEX
C10,C13	2	1.8pFHigh Q Capacitor	251SHS1R8BSE	TEMEX
C12	1	2.2pFHigh Q Capacitor	251SHS2R2BSE	TEMEX
R1	1	10Ω Power Resistor	ESR03EZPF100	ROHM
C5,C6,C7,C8	4	10uF MLCC	GRM32EC72A106ME05	Murata
T1	1	LDMOS Transistor	ITGV20080T2C	Innogration

Figure 2: Efficiency and power gain as function of Pout

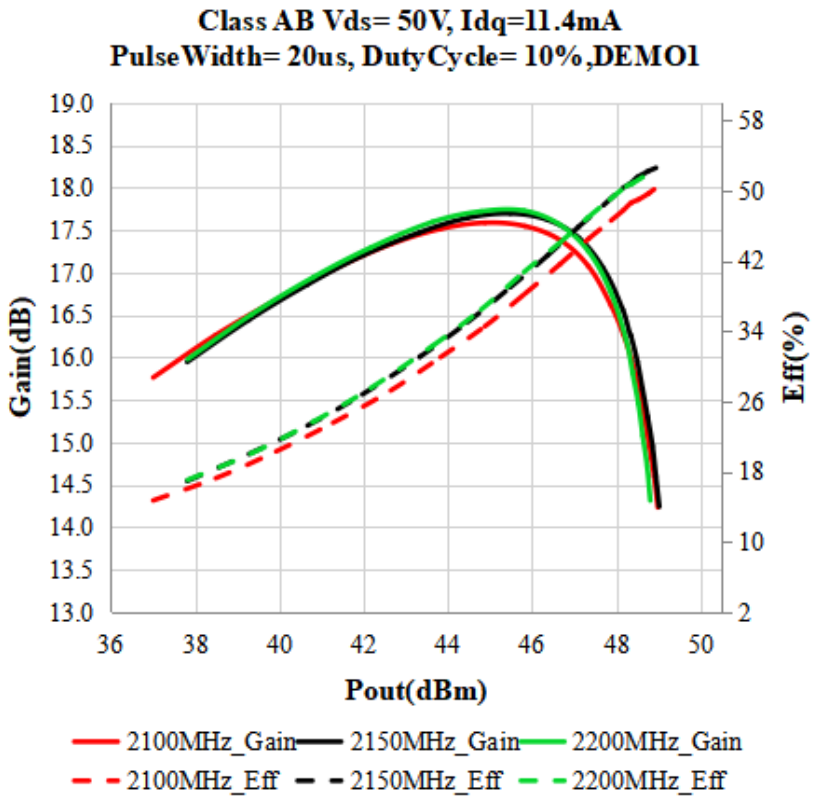
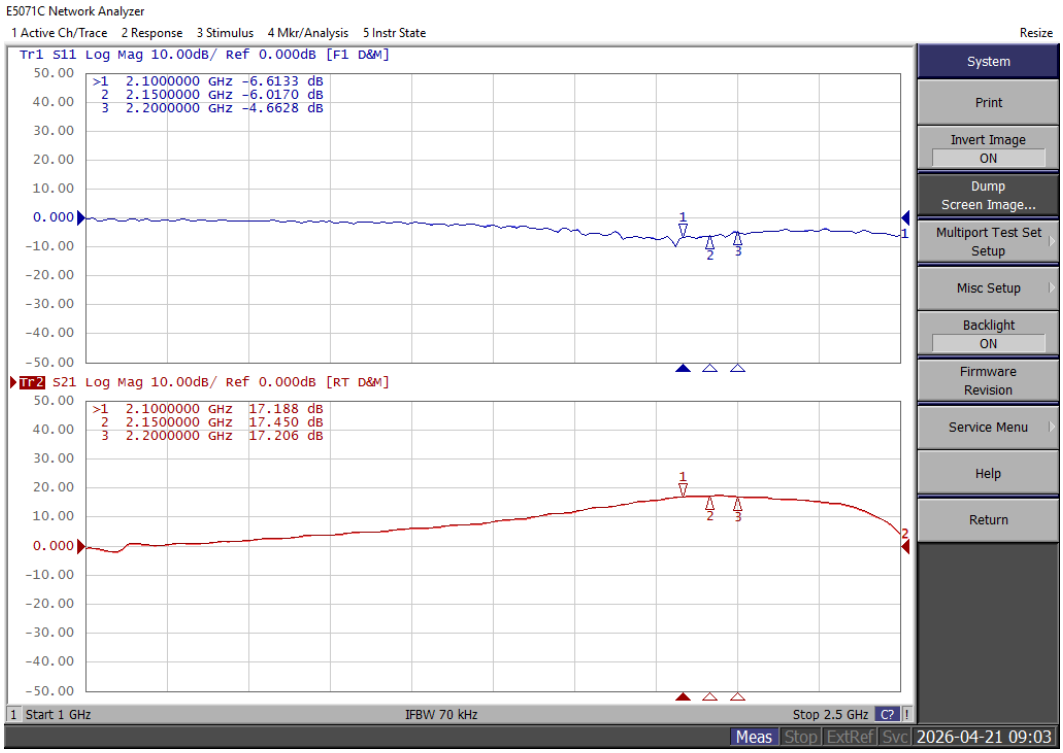


Figure 3: Small singal gain and return loss Vs Frequency



1800-1900MHz

Reference Circuit of Test Fixture Assembly Diagram

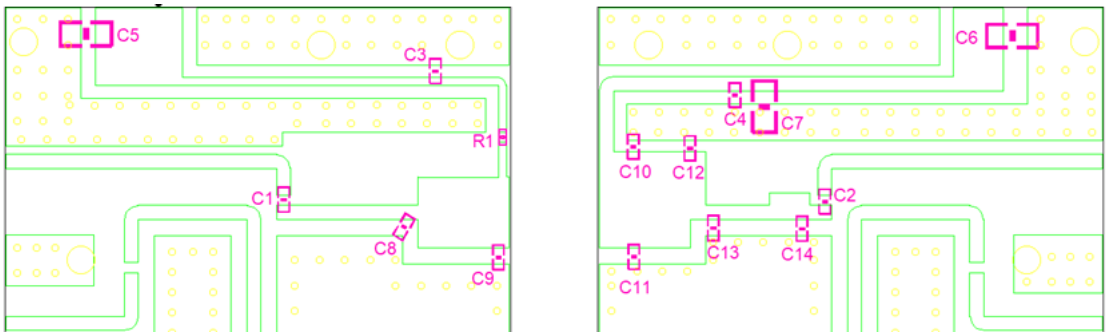


Figure 4. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Part	Quantity	Description	Part Number	Manufacture
C1	1	10pFHigh Q Capacitor	251SHS100BSE	TEMEX
C2,C3,C4	3	20pFHigh Q Capacitor	251SHS200BSE	TEMEX
C8	1	2.7pFHigh Q Capacitor	251SHS2R7BSE	TEMEX
C9,C10	2	1.8pFHigh Q Capacitor	251SHS1R8BSE	TEMEX
C11	1	3.0pFHigh Q Capacitor	251SHS3R0BSE	TEMEX
C12	1	0.4pFHigh Q Capacitor	251SHS0R4BSE	TEMEX
C13	1	3.9pFHigh Q Capacitor	251SHS3R9BSE	TEMEX
C14	1	0.2pFHigh Q Capacitor	251SHS0R2BSE	TEMEX
R1	1	10Ω Power Resistor	ESR03EZPF100	ROHM
C5,C6,C7	3	10uF MLCC	GRM32EC72A106 ME05	Murata
T1	1	LDMOS Transistor	ITGV20080T2C	Innogration

Figure 7: Efficiency and power gain as function of Pout

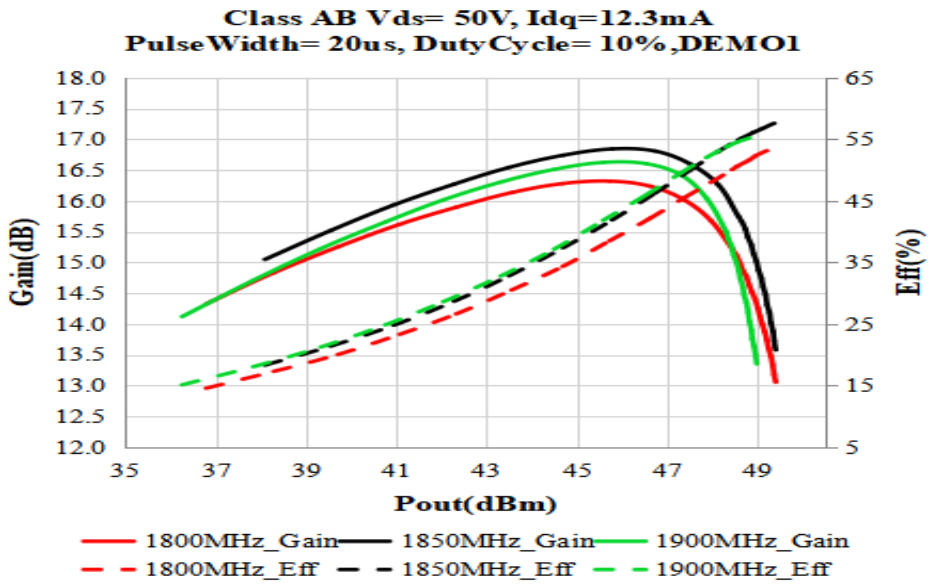
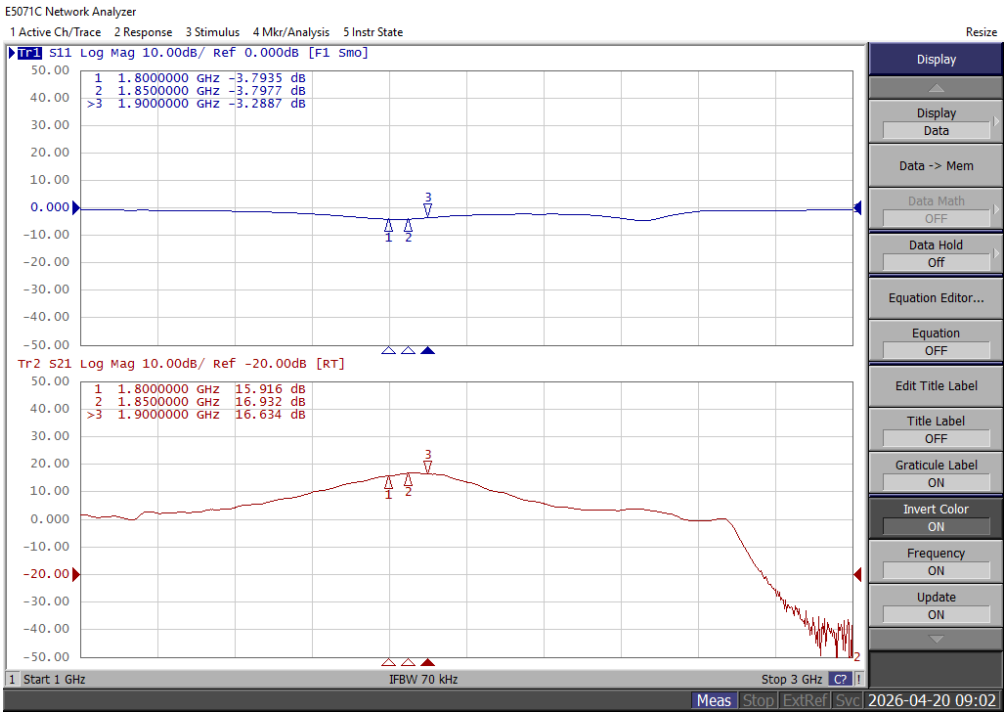


Figure 8: Small singal gain and return loss Vs Frequency



1400MHz

Reference Circuit of Test Fixture Assembly Diagram

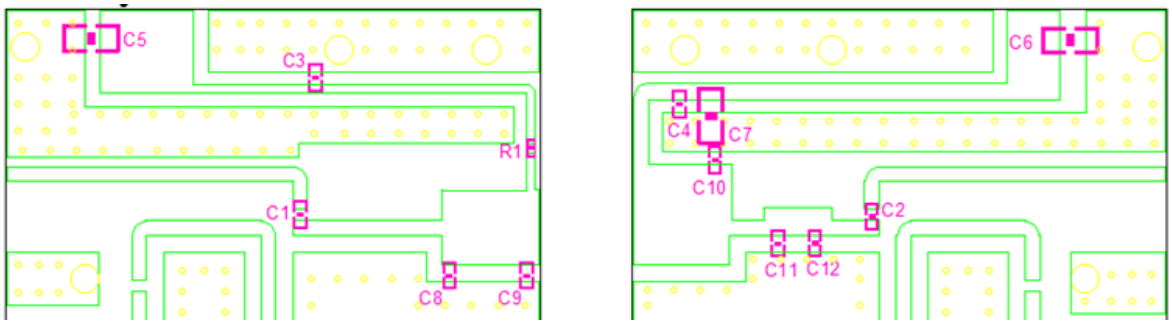


Figure 8 Test Circuit Component Layout

Table 7. Test Circuit Component Designations and Values

Part	Quantity	Description	Part Number	Manufacture
C1	1	3.9pFHigh Q Capacitor	251SHS3R9BSE	TEMEX
C2,C3,C4	3	33pFHigh Q Capacitor	251SHS330BSE	TEMEX
C8	1	6.2pFHigh Q Capacitor	251SHS6R2BSE	TEMEX
C9	1	3.6pFHigh Q Capacitor	251SHS3R6BSE	TEMEX
C10	1	0.2pFHigh Q Capacitor	251SHS0R2BSE	TEMEX
C11	1	5.6pFHigh Q Capacitor	251SHS5R6BSE	TEMEX
C12	1	0.6pFHigh Q Capacitor	251SHS0R6BSE	TEMEX
R1	1	10Ω Power Resistor	ESR03EZPF100	ROHM
C5,C6,C7	3	10uF MLCC	GRM32EC72A106ME 05	Murata
T1	1	LDMOS Transistor	ITGV20080T2C	Innogration

Figure 9: Efficiency and power gain as function of Pout

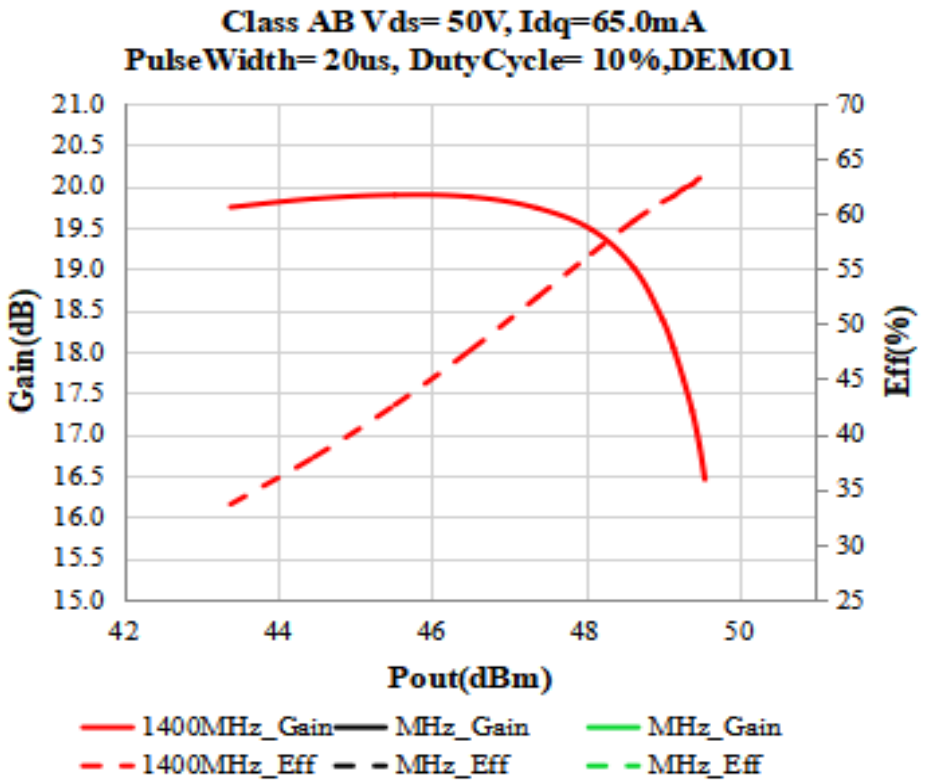
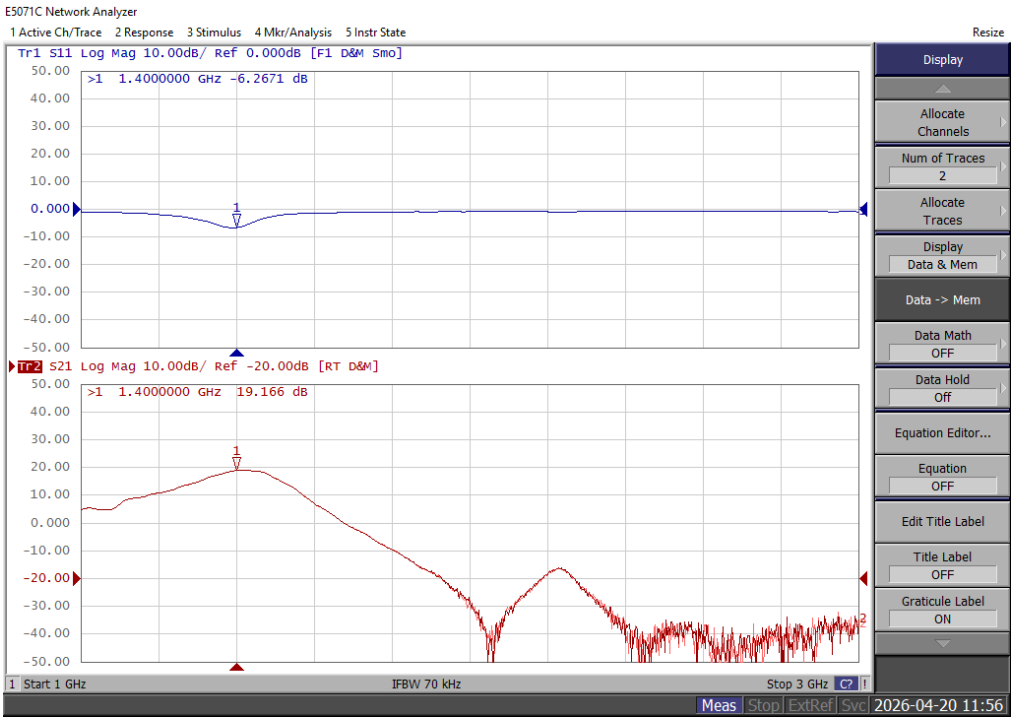


Figure 10: Small singal gain and return loss Vs Frequency

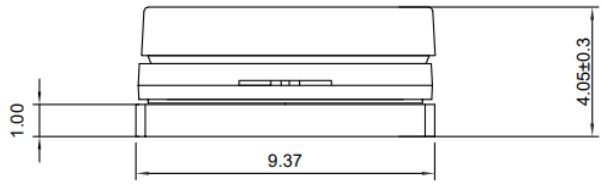


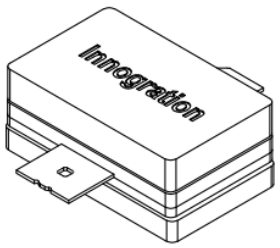
Package Outline

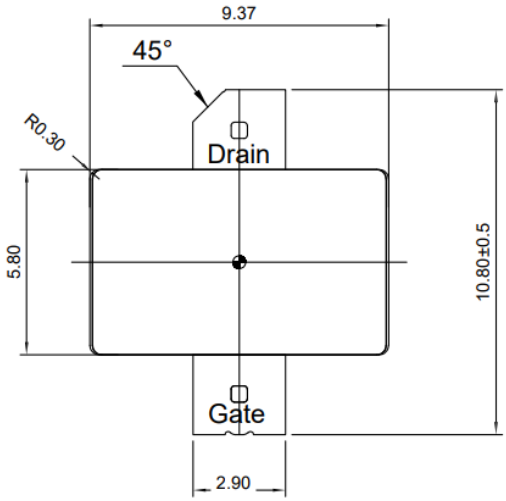
Flanged ceramic package; 2 leads

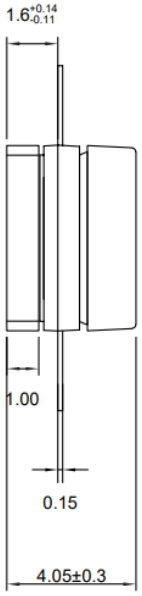
T2C POD

Rev.01 (2026.01.20)









Unit:mm
Tolerances(unless specified): x.x ±0.1

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-T2C/G2C					2018.1.31

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2026/4/21	Rev 1.0	Preliminary Datasheet

Application data based on HZH-26-12/13/14

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