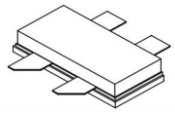
MK0930GS LDMOS TRANSISTOR

Document Number: MK0930GS
Product Datasheet V1.0

300W, P band High Power RF LDMOS FETs

MK0930GS



Description

The MK0930GS is a 300-watt,both input and output matched, high ruggedness，push pull LDMOS FETs, designed for P band and UHF application within 0.5 to 1GHz.

- Typical RF Performance under CW (On Innogration fixture with device soldered):

MK0930GS^{V0} VGS=2.45V VDS=28V IDQ=250mA CW								
Freq (MHz)	**Psat (dBm)**	**Psat (W)**	**IDS (A)**	**Pin (dBm)**	**Gain (dB)**	**Eff(%)**	**2nd （dBc）**	**3rd （dBc）**
600	54.48	280.5	15.68	41.10	13.38	63.90	-26.30	-65.80
650	54.87	306.9	16.87	41.20	13.67	64.97	-38.10	-56.60
700	54.74	297.9	17.01	41.15	13.59	62.54	-47.30	-52.90
750	54.62	289.7	16.72	41.20	13.42	61.89	-61.50	-44.50
800	54.95	312.6	17.60	41.70	13.25	63.44	-62.00	-52.80
850	55.08	322.1	17.12	42.00	13.08	67.20	-67.00	-49.30
910	54.18	261.8	13.16	41.00	13.18	71.05	-54.70	-49.80

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band pulse or CW amplifier
- UHF band pulsed amplifier
- Test measurement applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Tcase=25°C; CW	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

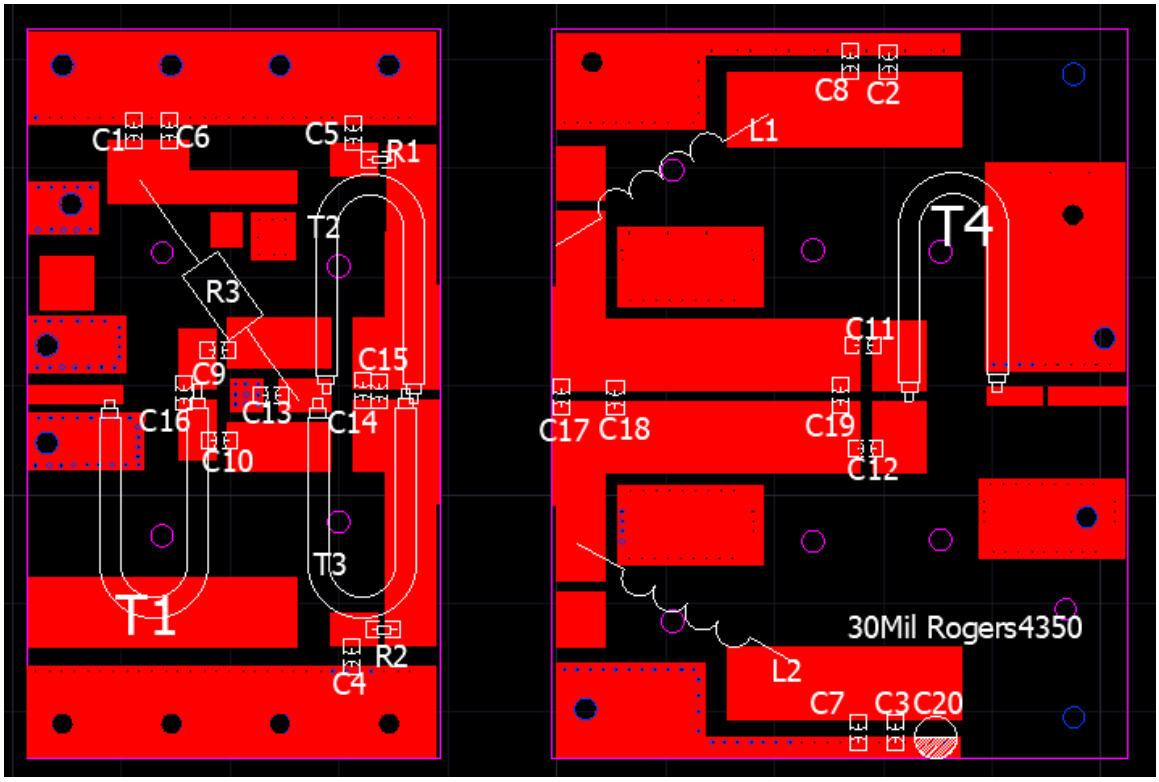
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 μA)	$V_{GS(th)}$		1.9		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 0.5A, Measured in Functional Test)	$V_{GS(Q)}$		2.5		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 1000 MHz

VSWR 5:1 at 300W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 2. Test Circuit Component Layout



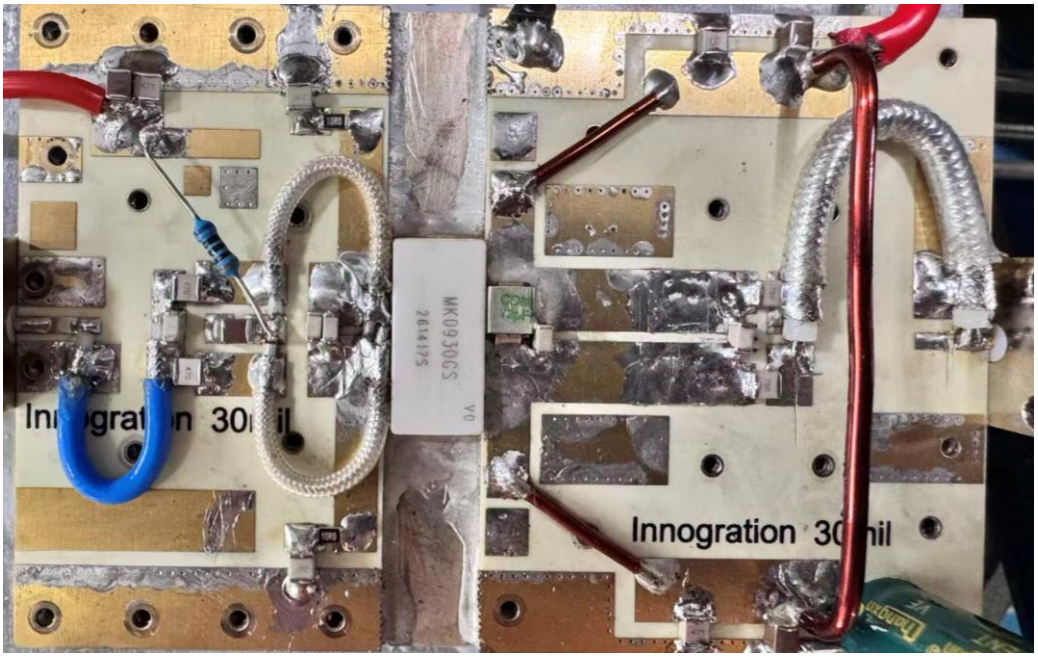
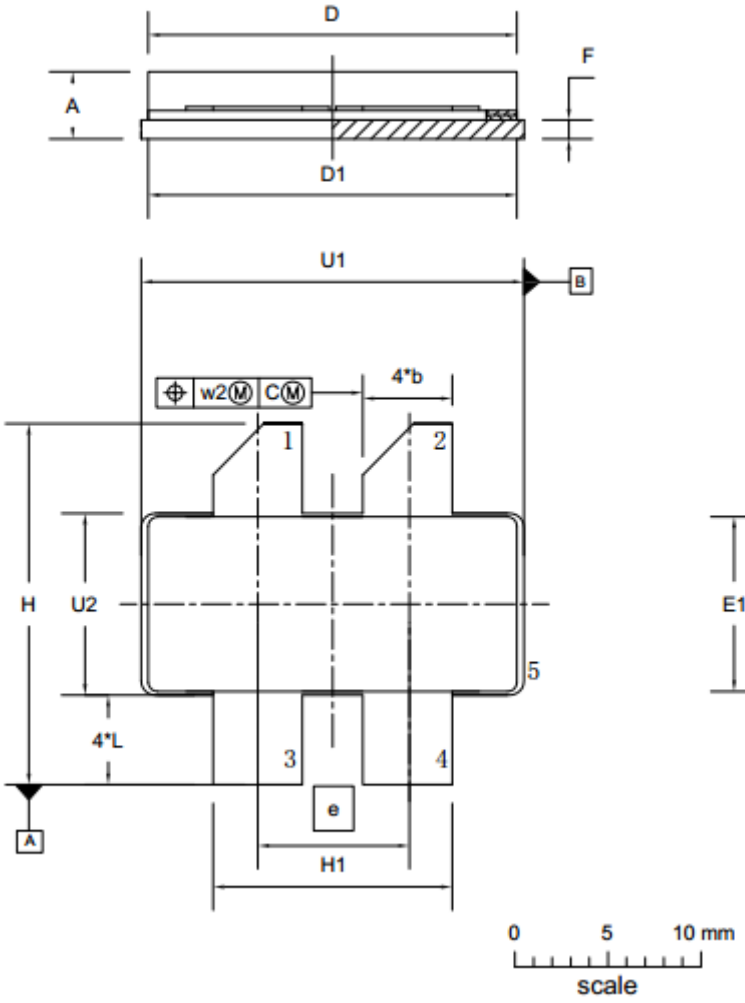


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1~C5,C13	10uF/200V-1210	Ceramic multilayer capacitor
C6~C8	470pF	
C9,C10	47pF	
C11,C12	75pF	
C14	6.8pF	
C15	3.9pF	
C16	1.5pF	
C17	12pF	
C18	4.3pF	
C19	5.1pF	
R1,R2	10Ω/1206	Chip Resistor
R3	300Ω	color ring resistor
T1	50 ohm-40mm	RFSFBU-086-50
T2,T3	16.7 ohm-40mm	SFF-16.7-1.5
T4	35ohm-55mm	SFF-35-3
L1,L2	1.5mm copper line	DIY

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/4/30	Rev 1.0	Product Datasheet

Application data based on TC-26-15

Disclaimers