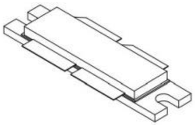
MQ012K4VPX LDMOS TRANSISTOR

Document Number: MQ012K4VPX
Preliminary Datasheet V1.1

2400W, 50V High Power RF LDMOS FETs

MQ012K4VPX



Description

The MQ012K4VPX is a 2400W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 150MHz

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

- Application data at multiple frequencies

Freq(MHz)	Voltage(V)/Idq(mA)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)	$2^{nd}/3^{rd}$（dB）
108	50/200	CW	46.4	2530	17.6	82	-30/-18
88-108	50/200	CW	43.5	1700	19	78	-25/-20

Features

- High breakdown voltage enable possible class E operation at lower Vdd
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	140	Vdc
Gate—Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 2400W CW, 50 Vdc, I_{DQ} = 240 mA	$R_{\theta JC}$	0.08	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.012	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage	$V_{(BR)DSS}$		140		V

V_{GS}=0V, I_{DS}=1.0Ma					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.9	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		110		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		1300		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		320		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		8		pF

TYPICAL CHARACTERISTICS (108MHz)

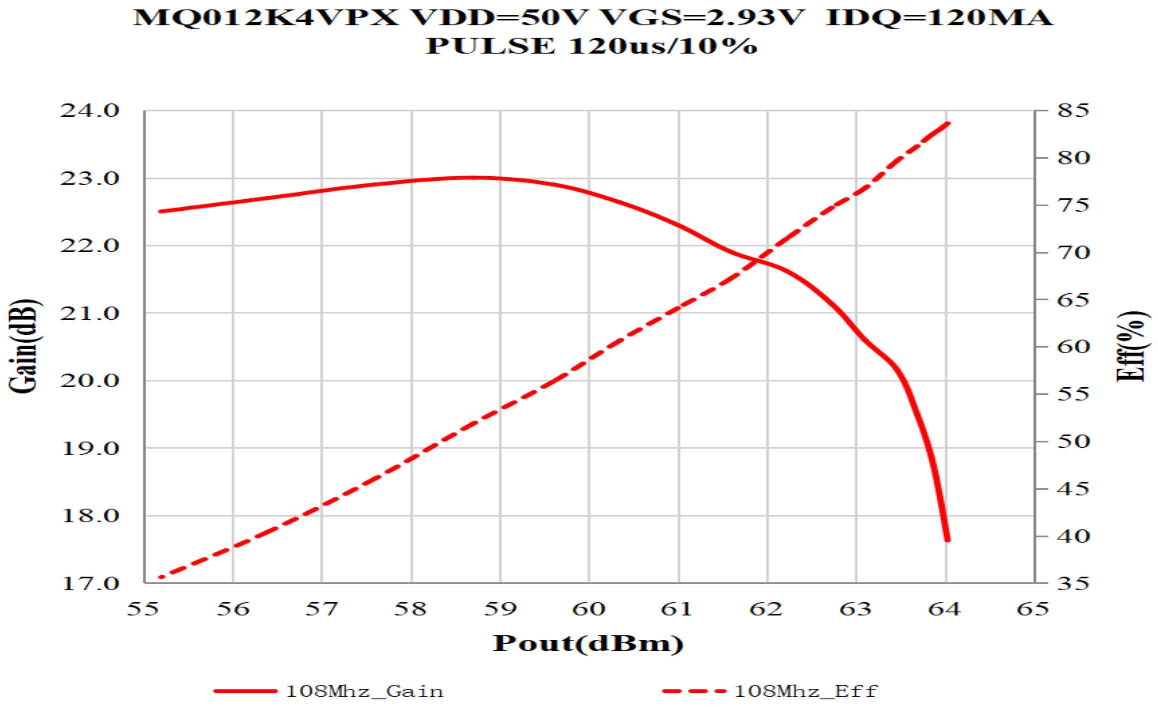


Figure 1: Efficiency and power gain as the function of Pout (Vds=50V, Idq=200mA)

Reference Circuit of Test Fixture (108MHz Power Amplifier)

Note: This demo board is used for short time demonstration only, for long time CW operation, heat management for some components might needed

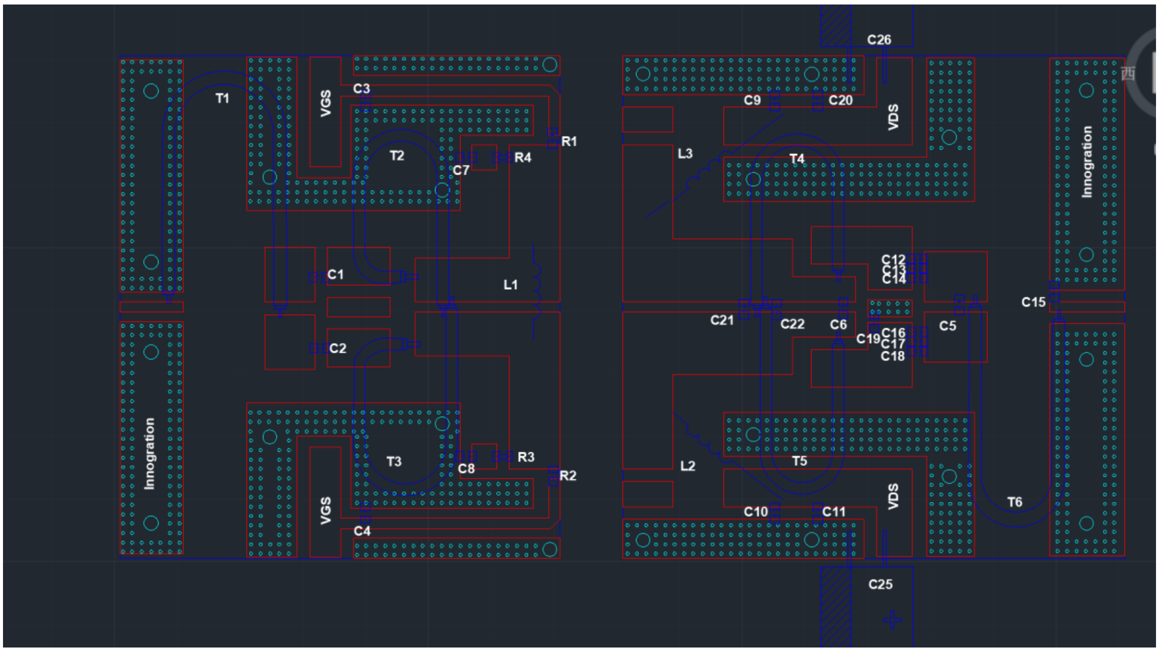
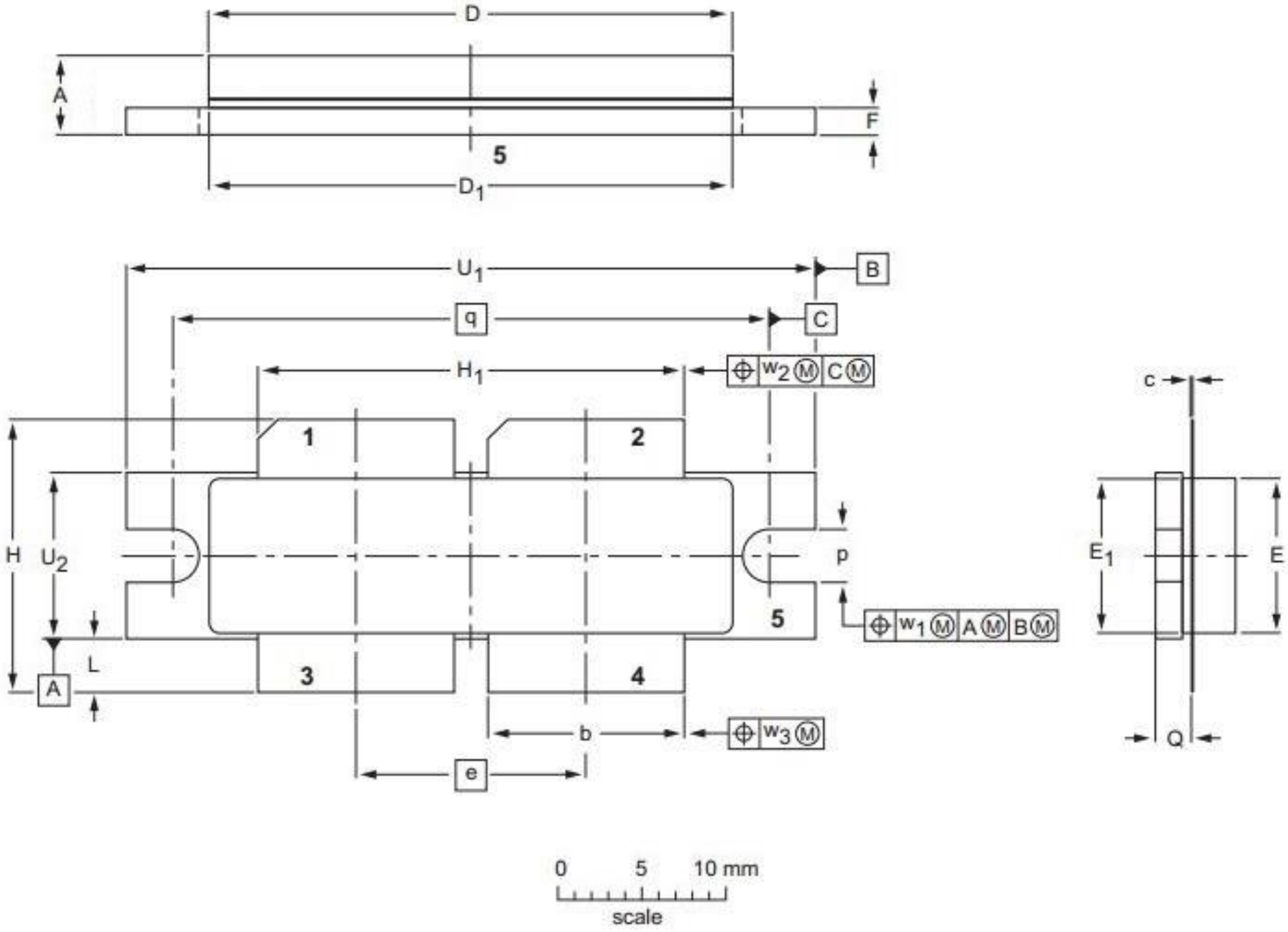


Table 5. Test Circuit Component Designations and Values

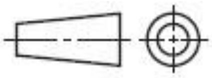
Component	Description	Suggestion
C1,C2	200pF/MQ101111	
C3,C4,C9,C10,C11,C20	10uF/1210	/
C5	24pF/MQ101111	
C6	15pF/MQ101111	
C7,C8	2.2uF/1210	
C12-C14,C16-C18	560pF/MQ101111	
C15	8.2pF/MQ101111	
C19	9.1pF/MQ101111	
C21	27pF/MQ101111	
C22	68pF/MQ101111	
R1,R2	360Ω	1206
R3,R4	10Ω	1206
T1	50 Ohm,200mm	RFSFBU-86-50
T2,T3	25 Ohm,150mm	SFF-25-1.5
T4,T5	12.5 Ohm,120mm	SFF-12.5-3
T6	35 Ohm,150mm	SFF-35-3
L1	0.8mm wire,1.2turns, Φ=3mm	DIY
L2,L3	2mm wire,6turns, Φ=5mm	DIY

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D₁	e	E	E₁	F	H	H₁	L	p	Q	q	U₁	U₂	W₁	W₂	W₂
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					**03/12/2013**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/11/28	Rev 1.0	Preliminary Datasheet
2026/4/7	Rev 1.1	Add FM 88-108MHz full band application dat

Application data based on SYX-25-57/HL-26-14

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