



# GaN 50V, 300W,4-5GHz RF Power Transistor

**STCV50W300D4**

## Description

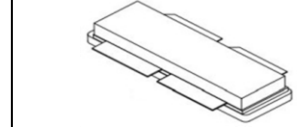
The STCV50W300D4 is a dual path 300watt capable, broadband GaN HEMT, ideal for ISM and Telecom especially CW applications within full band of 4-4GHz.

In typical 4.4-5GHz, It can deliver 300W CW with higher eff

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical CW performance at 4.4--5GHz applications

V<sub>DD</sub> = 50 Vdc, V<sub>GS</sub>=-3.55V, with device soldered, CW:



Freq (MHz)	Psat Gain(dB)	Psat (dBm)	Psat (W)	Idq (A)	Psat Eff(%)
4400	12.33	55.33	341	13.73	49.67
4500	13.2	55.13	326	12.17	53.57
4600	12.67	54.93	311	11.57	53.76
4700	11.68	54.80	302	12.15	49.71
4800	11.09	54.81	303	12.95	46.8
4900	11.06	54.94	312	13.33	46.81
5000	10.66	55.02	318	14.45	44.01

Recommended driver: STAV50061J2

## Applications

- C band power amplifier
- N79 mobile broadband

## Important Note: Proper Biasing Sequence for GaN HEMT Transistors

### Turning the device ON

1. Set V<sub>GS</sub> to the pinch--off (V<sub>P</sub>) voltage, typically -5 V
2. Turn on V<sub>DS</sub> to nominal supply voltage
3. Increase V<sub>GS</sub> until I<sub>DS</sub> current is attained
4. Apply RF input power to desired level

### Turning the device OFF

1. Turn RF power off
2. Reduce V<sub>GS</sub> down to V<sub>P</sub>, typically -5 V
3. Reduce V<sub>DS</sub> down to 0 V
4. Turn off V<sub>GS</sub>

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+200	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-8 to +0.5	Vdc
Operating Voltage	V <sub>DD</sub>	55	Vdc
Maximum gate current	I <sub>GS</sub>	50.4	mA
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>C</sub>	+150	°C
Operating Junction Temperature	T <sub>J</sub>	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T <sub>C</sub> = 25°C, at Pd=300W	R <sub>θJC</sub>	0.4	°C /W



**Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)**

**DC Characteristics (measured on wafer prior to packaging)**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=50.4mA	V <sub>DSS</sub>		200		V
Gate Threshold Voltage	VDS =10V, ID = 50.4mA	V <sub>GS(th)</sub>	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=700mA, Measured in Functional Test	V <sub>GS(Q)</sub>		--3.3		V

**Ruggedness Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	4.5GHz, Pout=300W pulse CW All phase, No device damages	VSWR		10:1		

## TYPICAL CHARACTERISTICS

**Figure 1: Efficiency and power gain as function of Pout (V<sub>DD</sub> = 50Vdc, V<sub>gs</sub>=-4.1V, Pulse width=20us, duty cycle=20%)**

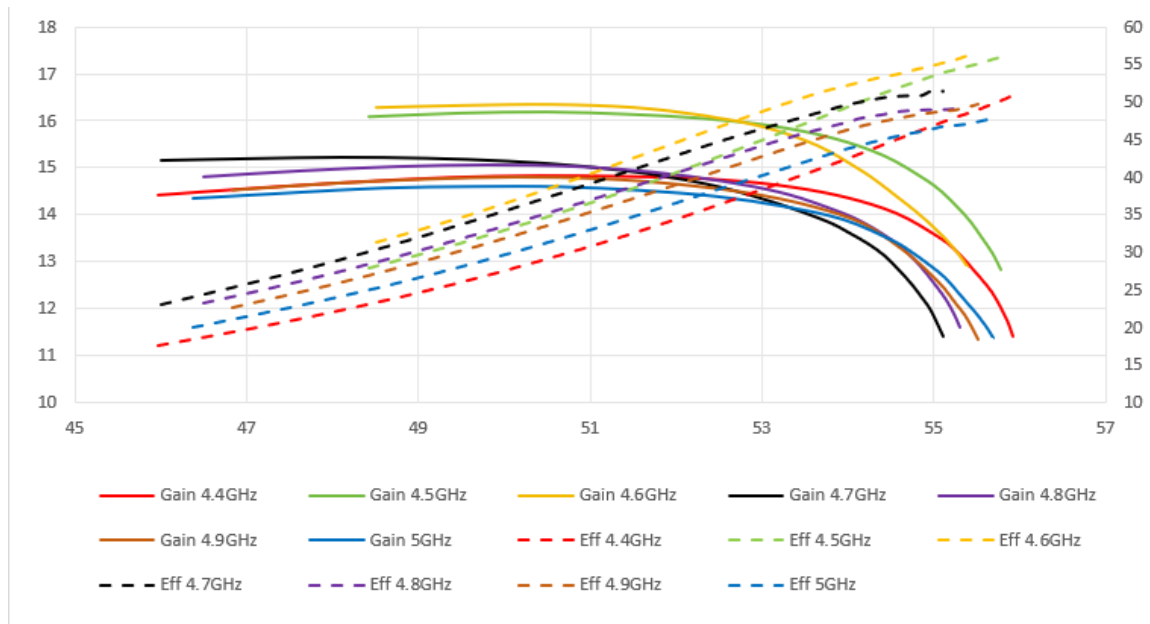
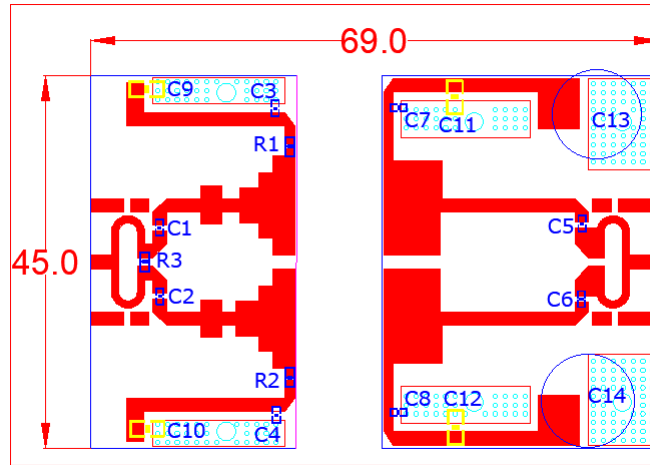


Figure 2: Reference design circuit (PCB DWG file upon request,)

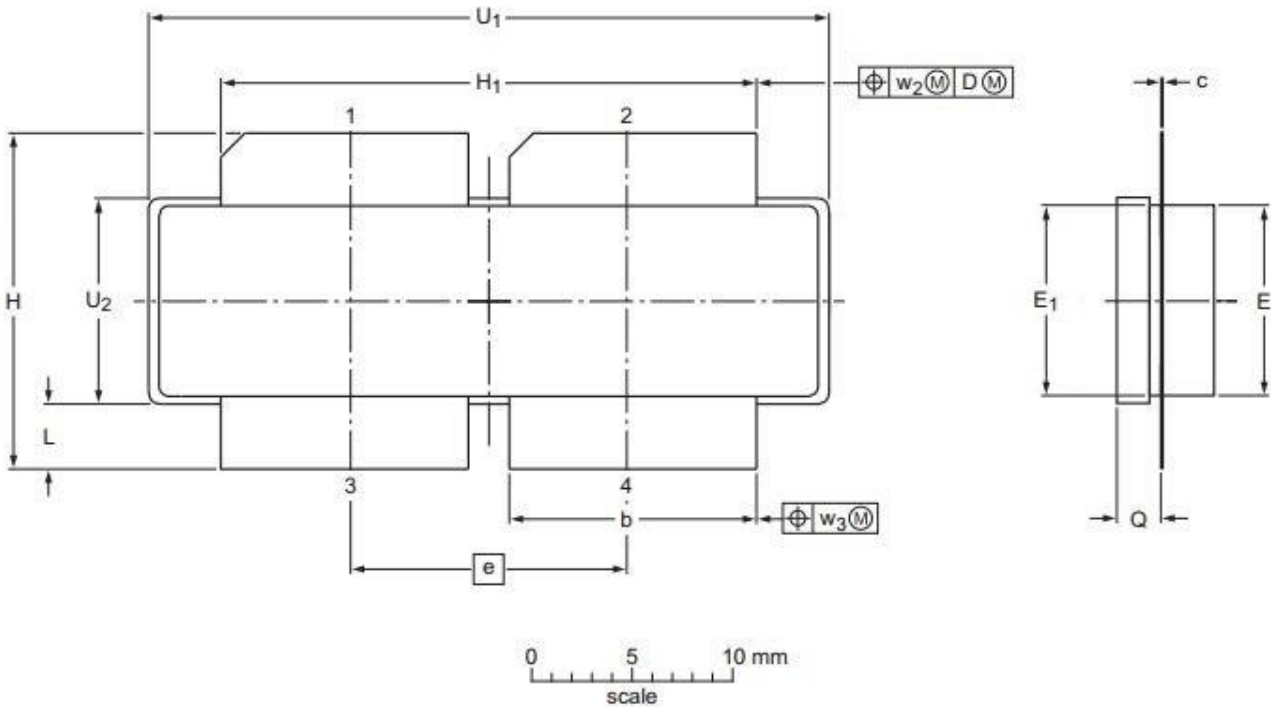
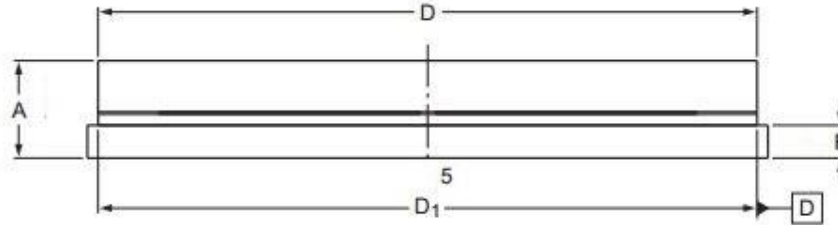


Part	Quantity	Description	Part Number	Manufacture
C1,C2,C3,C4,C5,C6	6	3.9pF High Q Capacitor	251SHF3R9BSE	TEMEX
C7,C8	2	1.5pF High Q Capacitor	251SHF1R5BSE	TEMEX
C9,C10,C11,C12,	4	10uF MLCC	RS80R2A106M	MARUWA
C13,C14	2	470uF		
R1,R2	2	10 Ω Power Resistor	ESR03EZPF100	ROHM
R3	1	100 Ω Power Resistor	ESR03EZPF100	ROHM
T1	1	GaN Transistor	STCV50W300D4	Innogrations



### Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>	W <sub>2</sub>
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/5/26	V1.0	Preliminary Datasheet Creation

Application data based on: LWH-26-13

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