



GaN HEMT 50V, 1200W, 0.6-1GHz RF Power Transistor

Description

The XTAV101K2RD4 is a 1200watt Doherty pair capable, GaN HEMT, ideal for for 4G/5G cellular applications up to 1GHz.

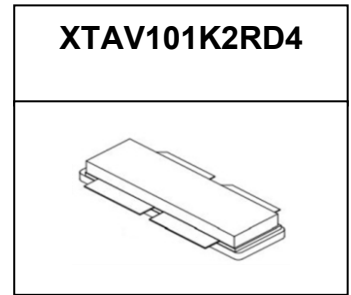
It can be configured as asymmetrical Doherty delivering 160-200W average power, according to normal 8-9dB back off.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on 758-803MHz Doherty

$V_{DD} = 48 \text{ Vdc}$, $I_{DQ_main} = 100\text{mA}$, $V_{gs_peak} = -5.5\text{V}$, 1 carrier WCDMA signal PAR=10.5dB

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Eff(%)
758	53	7.89	60.85	1216.3	-31.5	13.9	53
780	53	8.14	61.13	1295.9	-30.6	13.8	55
803	53	8.05	61.04	1269.9	-29.7	13.6	56



Applications

- Asymmetrical Doherty amplifier within <1GHz
- UHF TV
- P band communication

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

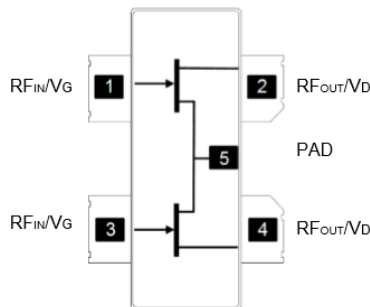


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc



Maximum gate current	I _{gs}	171	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T _c = 85°C, at Pd=160W, on Doherty application board	R _{θJC}	0.7	°C /W

Table 3. Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	700MHz, P _{out} =200W pulse CW for All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

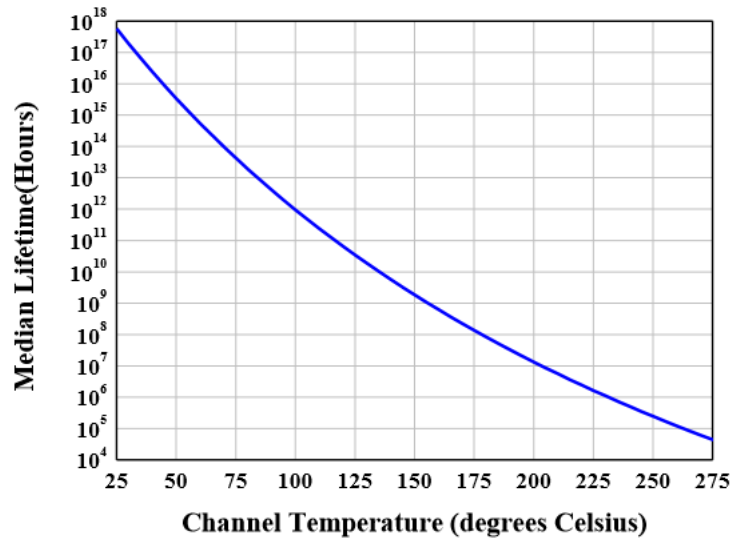




Figure 3: Efficiency and power gain as function of Pout (758-803MHz Doherty)

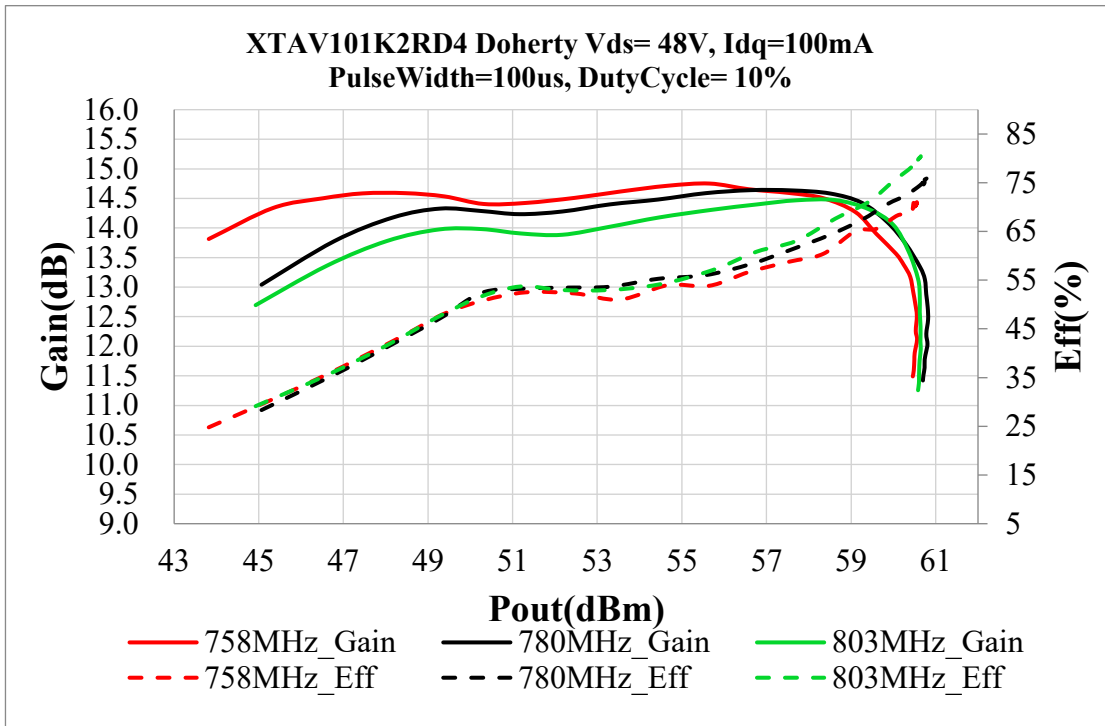


Figure 4: Network analyzer output, S11 and S21 (758-803MHz Doherty)

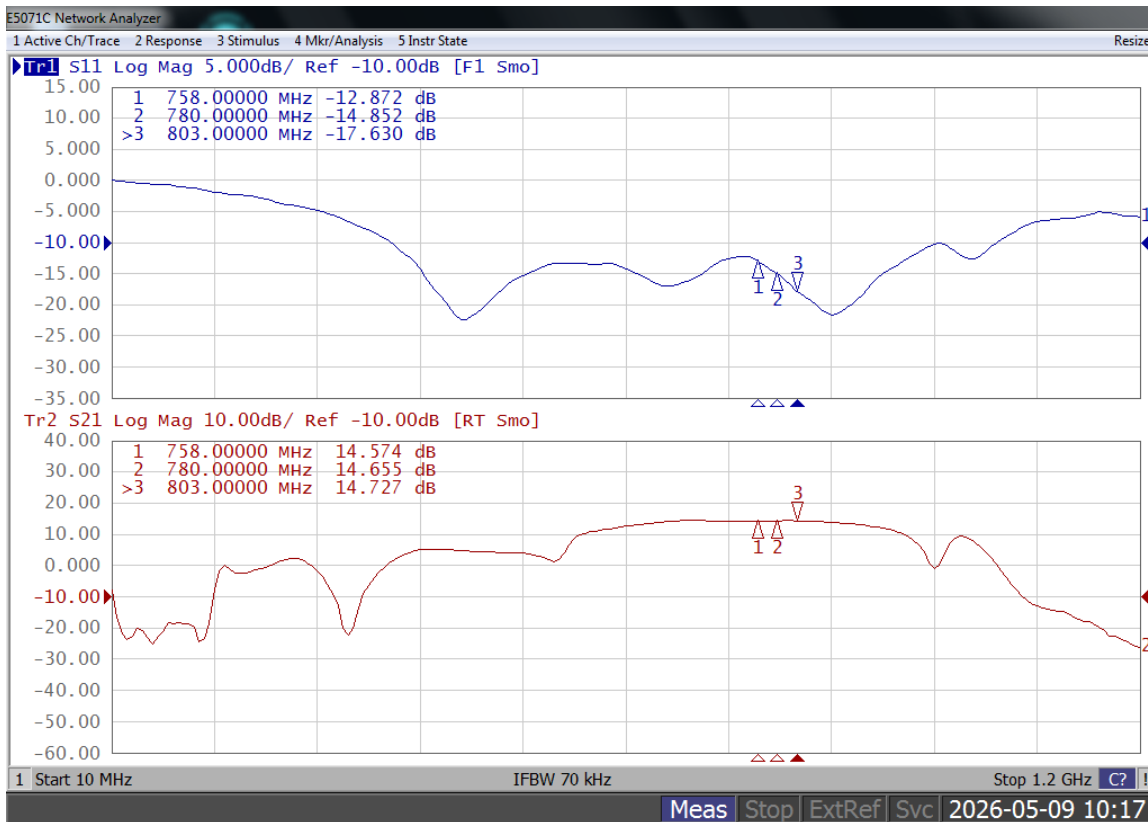


Figure 5: Picture of application board Doherty circuit for 758-803MHz

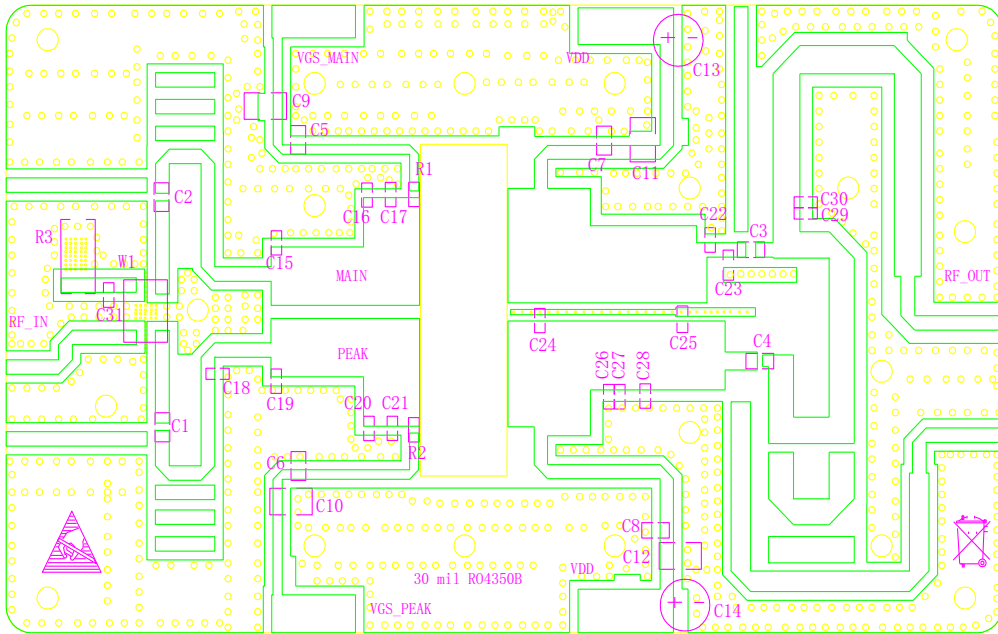


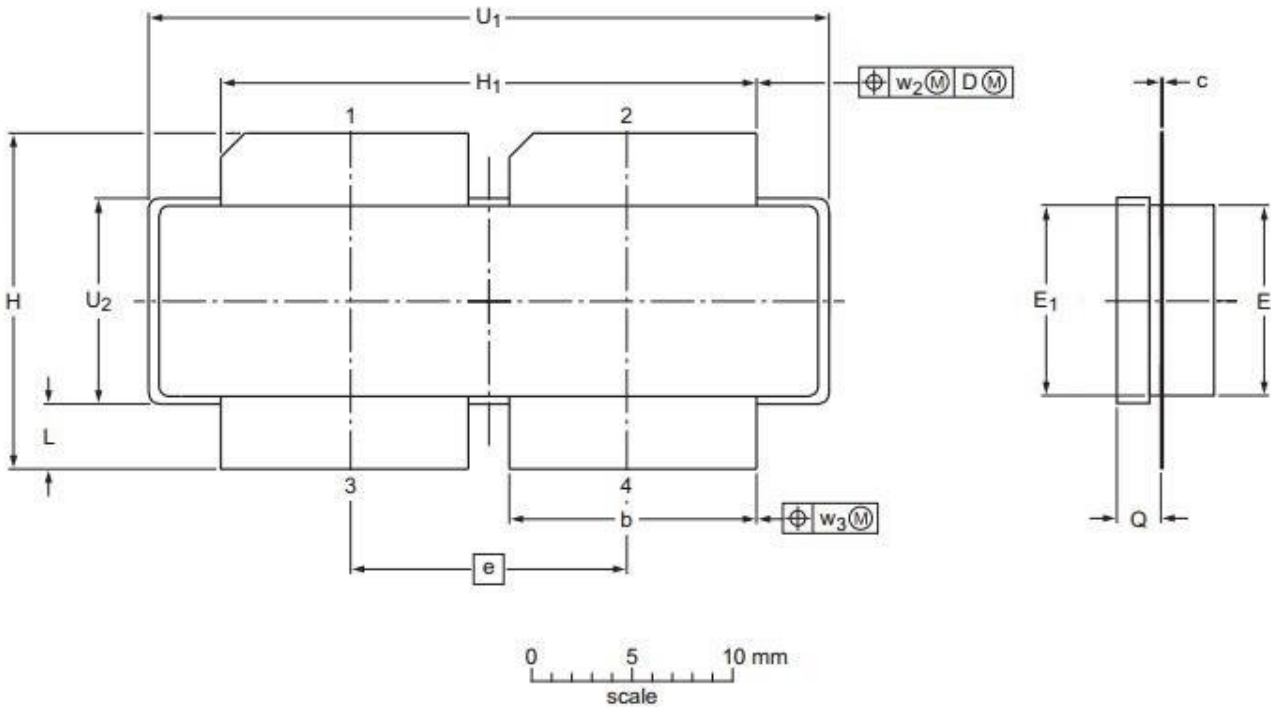
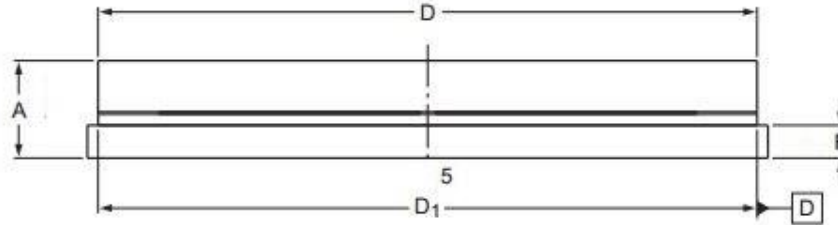
Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 30mils)

Designator	Footprint	Comment	Quantity
C1, C2, C22, C23, C25, C26, C27, C28	0805	6.8pF	8
C3, C4, C5, C6, C7, C8	0805	68pF	6
C9, C10, C11, C12	1210	10uF/100V	4
C13, C14		470uF/63V	2
C15, C16, C17, C19, C20, C21	0603/0805	20 pF	6
C18, C24	0603/0805	2 pF	2
C29, C30	0805	1.0pF	2
C31	0603/0805	1.5 pF	1
R1, R2	0603	10R	2
R3		RFR50N-20 CT0410B	1
W1		DC07F02	1



Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/5/9	V1.0	Preliminary Datasheet Creation

Application data based on:LSM-26-12

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