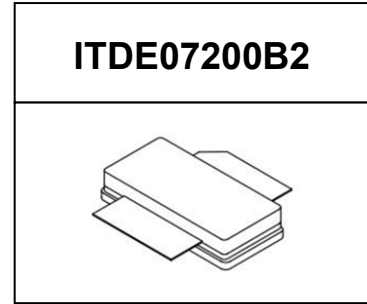




200W, 28V High Power RF LDMOS FETs



Description

The ITDE07200B2 is a 200-watt, internally matched LDMOS FETs, designed for multiple applications with frequencies within HF to UHF

It can be used in Class AB/B and Class C to support CW,Pulsed CW or any modulation Signal.

•Typical Performance (On Innegration fixture with device soldered)

VDD = 28 Volts, Idq=100mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
450	53.77	237	65.89	18.7	54.44	277	68.92
460	53.33	215	68.39	19.1	54.01	251	71.24
470	52.50	177	68.35	18.9	53.30	213	71.69

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCl drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+95	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test	R _{θJC}	0.34	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage	V _{(BR)DSS}	95	—		V



$V_{GS}=0, I_{DS}=1.0mA$					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75V, V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28V, V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10V, V_{DS} = 0V$)	I_{DSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28V, I_D = 300\mu A$)	$V_{GS(th)}$	—	2.15	—	V
Gate Quiescent Voltage ($V_{DD} = 28V, I_D = 1000mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.2	—	V

Functional Tests (In Demo Test Fixture, 50 ohm system) $V_{DD} = 28Vdc, I_{DQ} = 100mA, f = 700MHz$, Pulse Width =10us, Duty Cycle =10%..

Power Gain	G_p	—	14	—	dB
Drain Efficiency@P3dB	η_D	—	60	—	%
3 dB Compression Point	P_{-3dB}	—	200	—	W
Input Return Loss	IRL	—	-5	—	dB

Load Mismatch (In Innogrations Test Fixture, 50 ohm system): $V_{DD} = 28Vdc, I_{DQ} = 100mA, f = 700MHz$

VSWR 10:1 at 200W pulse CW Output Power	No Device Degradation
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450MHz application board

Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

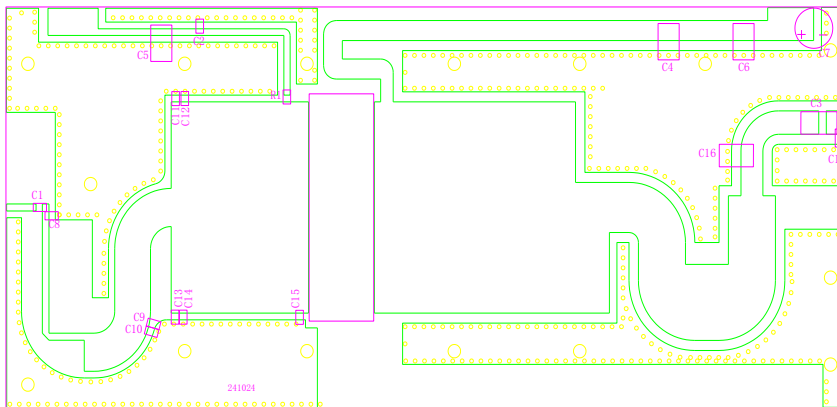


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

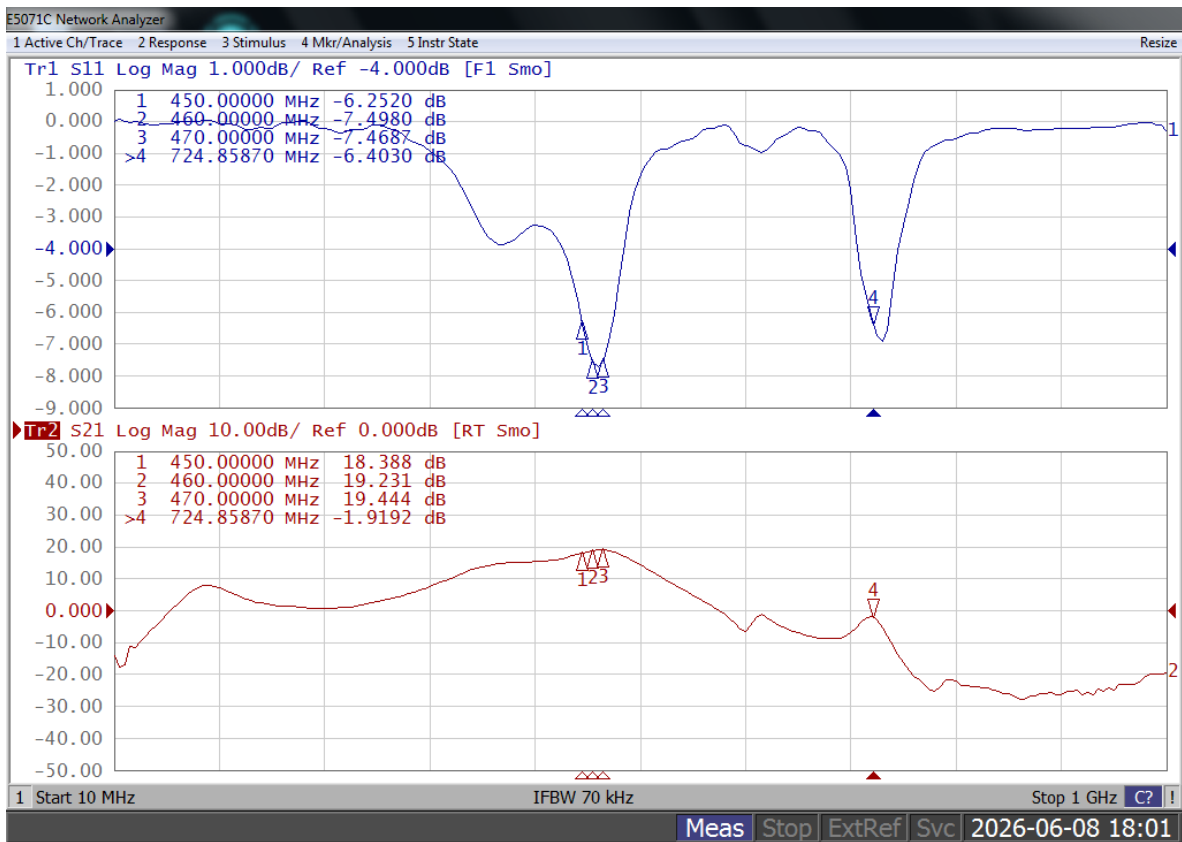
Designator	Comment	Footprint	Quantity
C1, C8, C9, C10	10 pF	0805	4
C2	100 pF	0805	1
C3, C4	100 pF	1210	2
C5, C6	10uF/100V	1210	2



C7	1000uF/63V		1
C11, C12, C13, C15	30 pF	0805	4
C14	15 pF	0805	1
C16	1.0pF	1210	1
C17	6.8 pF	0805	1
R1	10 Ω	0603	1

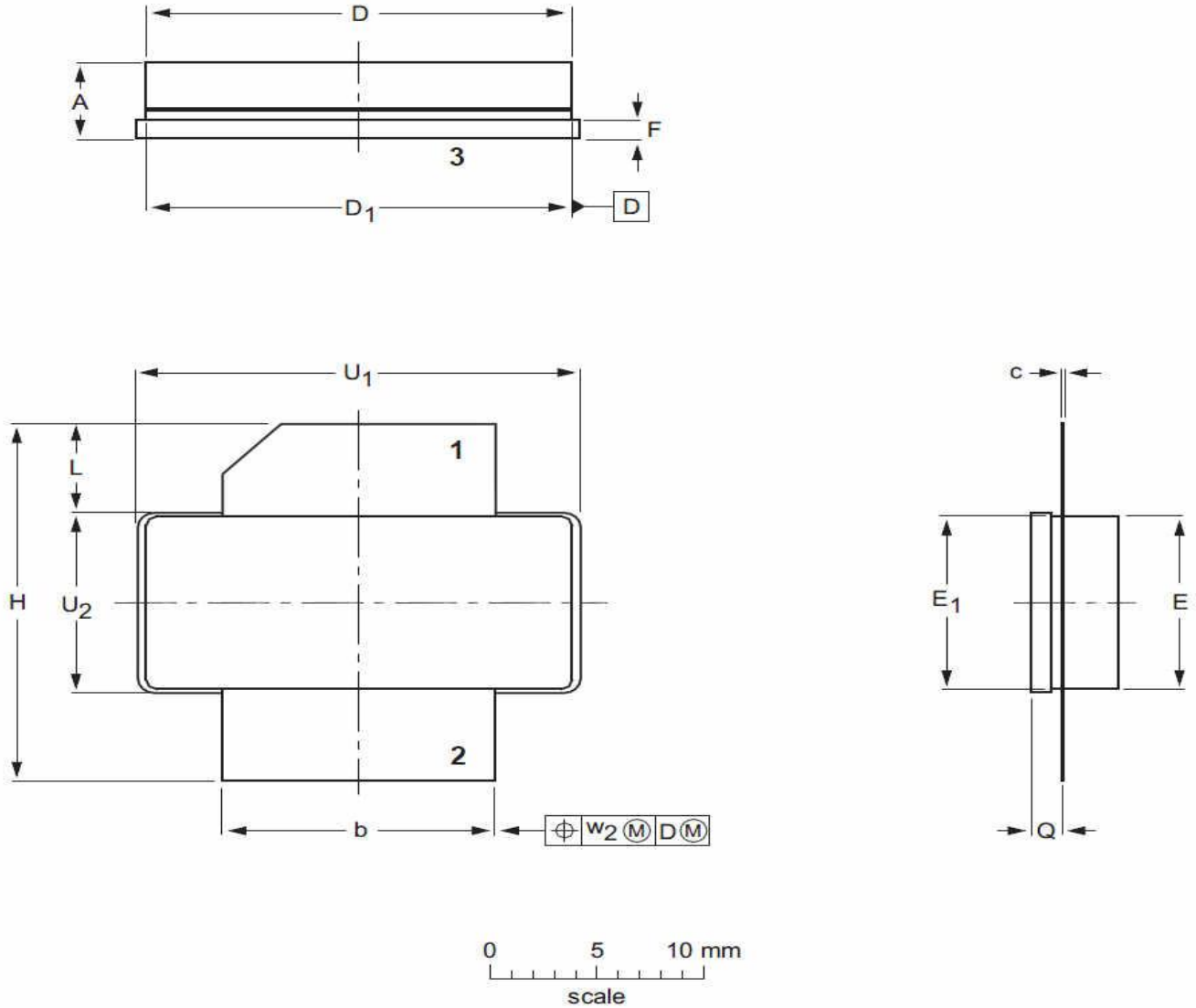
TYPICAL CHARACTERISTICS

Figure 3. Network analyzer output S11/S21





Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/6/9	Rev 1.0	Product Datasheet

Application data based on LSM-26-19

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