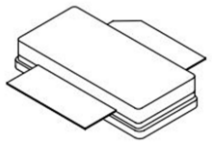
160W, 28V High Power RF LDMOS FETs

ITDE07160B2



Description

The ITDE07160B2 is a 160-watt, internally matched LDMOS FETs, designed for multiple applications with frequencies within HF to UHF

It can be used in Class AB/B and Class C to support CW,Pulsed CW or any modulation Signal.

•Typical Performance (On Innogration fixture with device soldered)

VDD = 28 Volts, Idq=100mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
450	52.53	179.0	66.5	18.67	53.21	209.5	71.1
460	52.26	168.4	69.3	19.07	52.9	195.1	72.7
470	51.79	151.0	70.1	18.99	52.47	176.6	73.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.45	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage	$V_{(BR)DSS}$	95	——		V

V_{GS}=0, I_{DS}=1.0mA					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 300 μA)	$V_{GS(th)}$	——	2.15	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 1000 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 100mA, f = 700 MHz, Pulse Width =10us, Duty Cycle =10%..

Power Gain	Gp	——	15	——	dB
Drain Efficiency@P3dB	η_D	——	65	——	%
3 dB Compression Point	P_{-3dB}	——	160	——	W
Input Return Loss	IRL	——	-5	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 700 MHz

VSWR 10:1 at 160W pulse CW Output Power	No Device Degradation

450MHz application board

Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

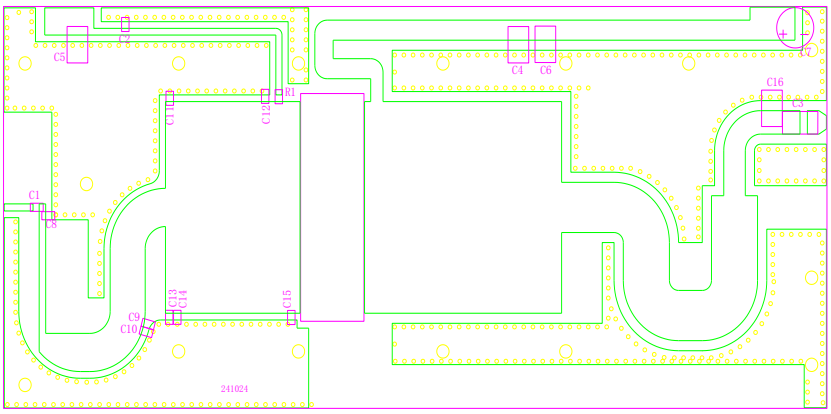


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1, C8, C9, C10	10 pF	0805	4
C2	100 pF	0805	1
C3, C4	100 pF	1210	2
C5, C6	10uF/100V	1210	2
C7	1000uF/63V		1

C11, C12, C13, C14, C15	30 pF	0805	4
C16	5.6 pF	0805	1
R1	10 Ω	0603	1

TYPICAL CHARACTERISTICS

Figure 3.Network analyzer output S11/S21

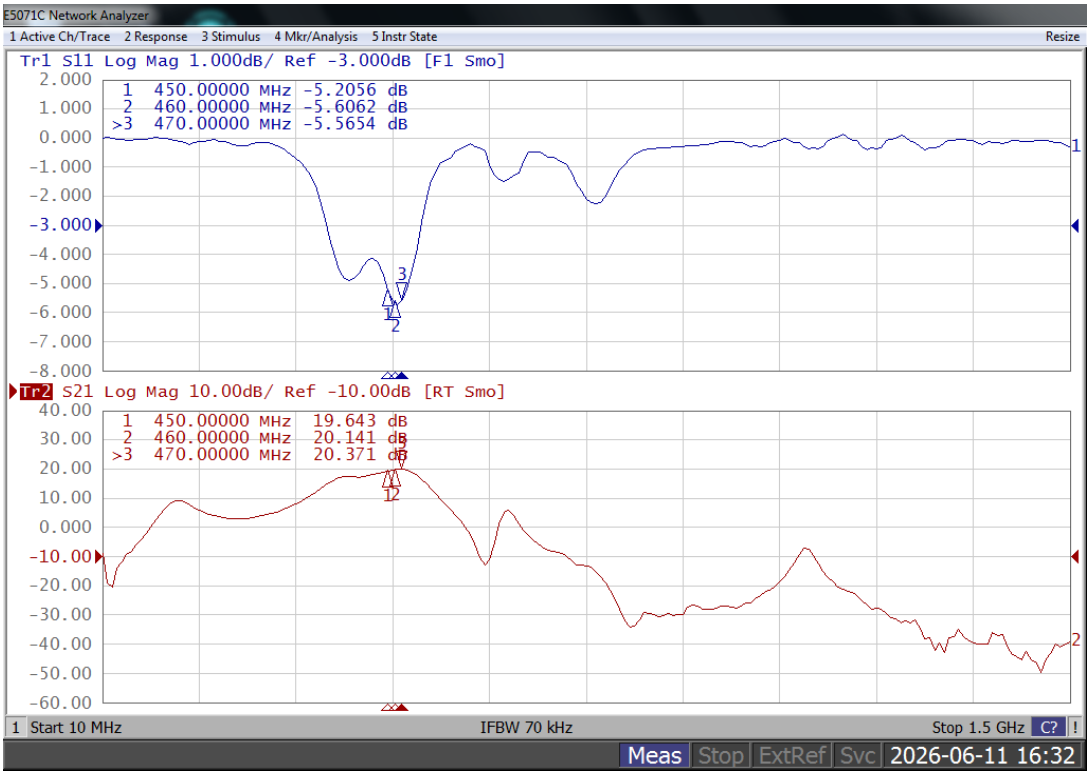
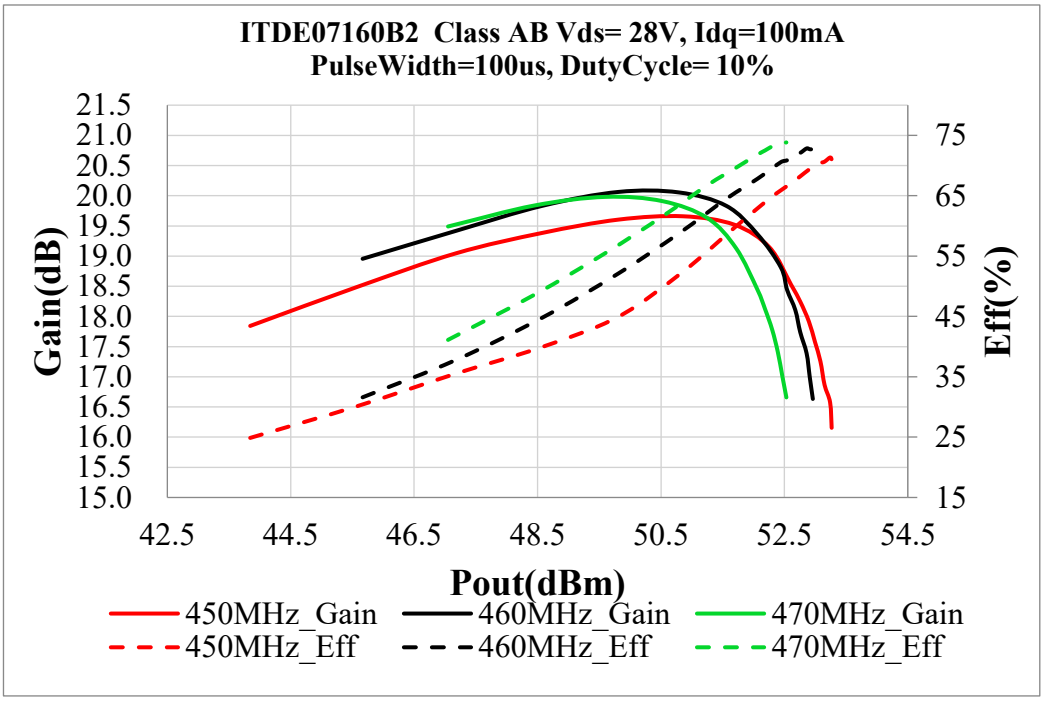
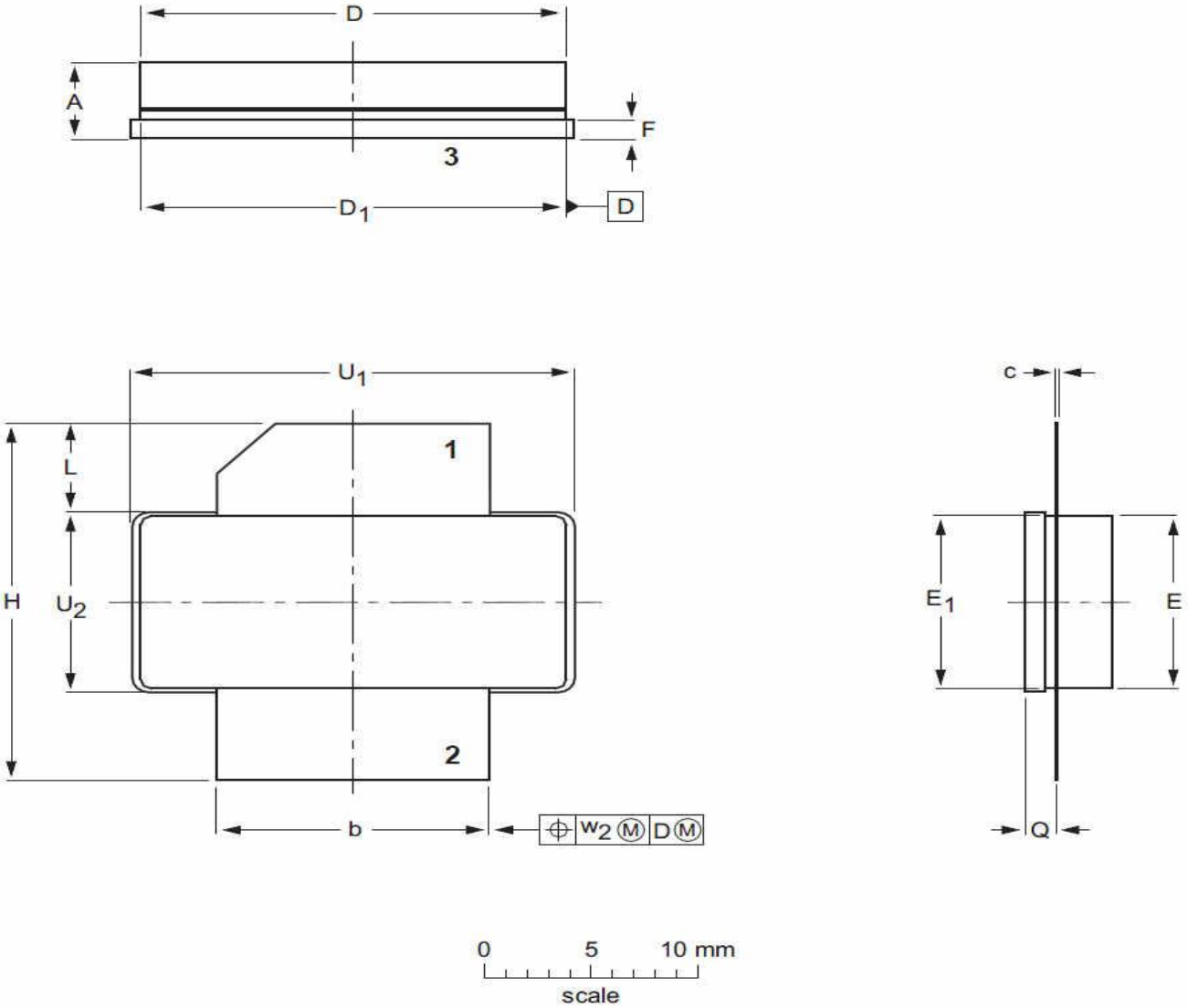


Figure 4.Network analyzer output S11/S21



Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/6/11	Rev 1.0	Product Datasheet

Application data based on LSM-26-20

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