

M2Q1062VPS LDMOS TRANSISTOR

Document Number: M2Q1062VPS
Preliminary Datasheet V1.0

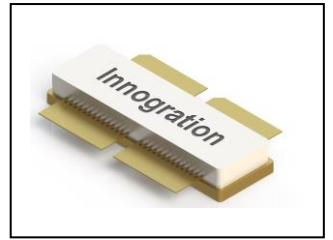
600W, UHF band 50V High Power RF LDMOS FETs

Description

The M2Q1062VPS is a 600W capable, Input/Output matched LDMOS FET, designed for commercial and industrial applications within UHF band up to 1GHz, supporting both pulse and CW applications upon bandwidth trade off. **In typical 400-700M full band tuning, it can reach >500W CW power with higher efficiency**

It can be taken as the bandwidth expansion of M2Q1060RVP

There isn't guarantee when this device is used outside of the band stated above.



- Typical RF performance within 400-1000MHz with device soldered

M2Q1062VPS ^{V0} VGS=3.07V VDS=50V IDQ=160mA CW								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff(%)	2nd (dBc)	3rd (dBc)
400	57.75	595.7	17.60	42.45	15.30	67.69	-28.50	-22.00
450	57.91	618.0	19.20	42.50	15.41	64.38	-25.00	-21.20
500	58.14	651.6	20.85	42.88	15.26	62.51	-21.70	-19.00
550	58.07	641.2	20.84	42.14	15.93	61.54	-31.50	-33.10
600	57.64	580.8	18.96	41.67	15.97	61.26	-31.40	-36.60
650	57.43	553.4	18.12	42.71	14.72	61.08	-36.80	-48.70
700	57.32	539.5	17.48	42.60	14.72	61.73	-35.30	-41.40

Features

- High breakdown voltage enable high ruggedness
- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	110	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 25°C, 50Vdc, DC test	R _{θJC}	0.26	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
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Human Body Model (per JESD22--A114)	Class 2
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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0V, I _{DS} =1.0mA	V _{(BR)DSS}		110		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate—Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 μA)	V _{GS(th)}	—	2.54	—	V
Gate Quiescent Voltage (V _{DD} = 50 V, I _D = 900 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.3	—	V

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400-700MHz

Reference Circuit of Test Fixture
(Layout file upon request) PCB: Roger 4350B, 30mils



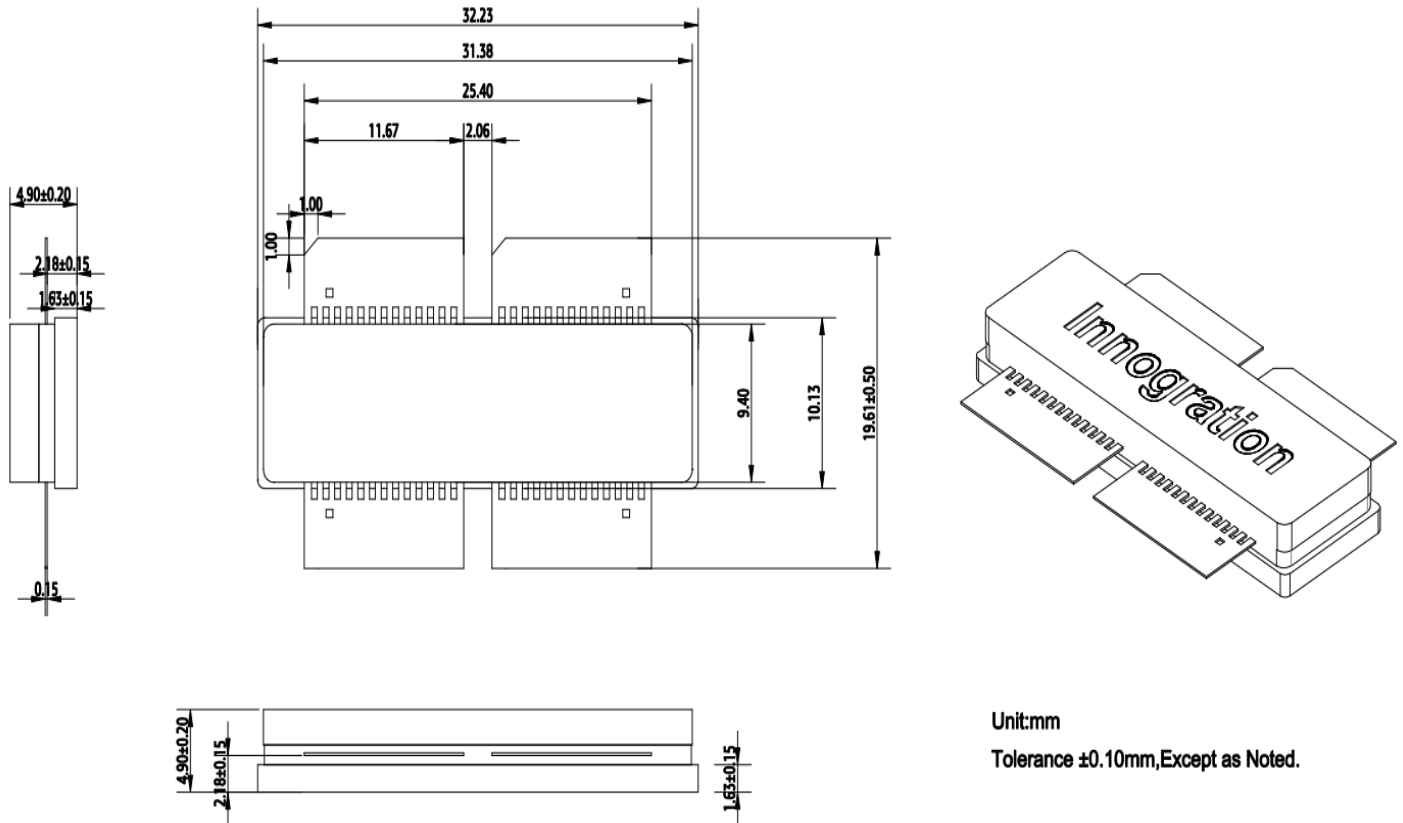
Component	Description	Suggested Manufacturer
C1~C5,C17,C18	10uF/200V-1210	Ceramic multilayer capacitor
C6~C8	470pF	
C9,C10	1000pF	
C11,C12	39pF	
C13~C16	47pF	
C19	20pF	
C20	5.1pF	
C21	12pF	
C22	1.5pF	
C23	2pF	
C24	5.6pF	
C25	10pF	
C26	3pF	
R1,R2	10 Ω /1206	Chip Resistor
R3	300 Ω	color ring resistor
R4,R5	300 Ω	RFT-300
R6	10 Ω *3/1206	Chip Resistor
T1	50 ohm-40mm	RFSFBU-086-50
T2,T3	16.7 ohm-40mm	SFF-16.7-1.5
T4,T5	16.7 ohm-50mm	SFF-16.7-1.5
T6	35 ohm-50mm	SFF-35-3
L1,L2	1.5mm wire	DIY

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Package Outline

Earless Flanged Plastic Air Cavity Package; 4 leads



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/7/24	Rev 1.0	Preliminary Datasheet

Application data based on TC-26-26

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