



20W,28V Plastic RF LDMOS Transistor

ITEH09020C6

Description

The ITEH09020C6 is a dual path 20-watt, symmetrical, highly rugged, LDMOS transistor, designed for low power applications at frequencies from 0.6 to 1.0GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as highly compact Doherty ,ideal for high efficiency and low cost, DPD friendly driver for 4G/5G application within 0.6-1.0GHz.



- Typical 600MHz Doherty RF Performance (On Innegration fixture with device soldered).

V_{ds}=28V Id_{q_main}=30mA, V_{gs_peak}=0.9V

@35dBm_1C-WCDMA							
Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
578	35.00	8.80	43.80	24.0	-28.6	19.2	50.5
628	35.00	9.14	44.14	26.0	-33.6	19.0	51.3
678	35.00	8.78	43.77	23.9	-36.6	18.3	49.5

- Typical 700MHz Doherty RF Performance (On Innegration fixture with device soldered).

V_{ds}=28V Id_{q_main}=30mA, V_{gs_peak}=0.9V

@35dBm_1C-WCDMA							
Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
758	35.01	8.34	43.34	21.6	-28.5	17.9	53.2
788	34.99	8.23	43.22	21.0	-31.7	17.8	52.1
803	35.00	8.20	43.20	20.9	-33.8	17.8	51.2

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band power amplifier
- All 4G/5G cellular application within 0.6 to 1.0GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DO}	+28	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C



Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^{\circ}\text{C}$, $T_J = 200^{\circ}\text{C}$, DC test	$R_{\theta JC}$	0.9	$^{\circ}\text{C/W}$

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

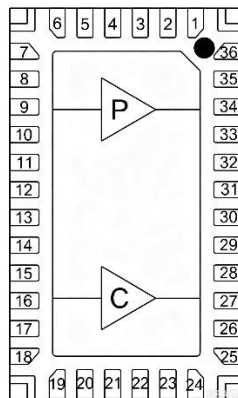
Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 100\mu\text{A}$	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 28\text{V}$, $I_D = 30\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.63	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 28\text{Vdc}$, $I_{DQ} = 180\text{mA}$, $f = 2200\text{MHz}$

VSWR 10:1 at 40W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9,10,11	RF IN/Vgs1	RF Input, Vgs bias for peak path
14,15,16,17	RF IN/Vgs2	RF Input, Vgs bias for main path
32,33,34,35	RF OUT/VDD1	RF Output, VDD bias for peak path
26,27,28,29	RF OUT/VDD2	RF Output, VDD bias for main path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

578-678MHz application board

Reference Circuit of Test Fixture Assembly Diagram

20mils RO4350B

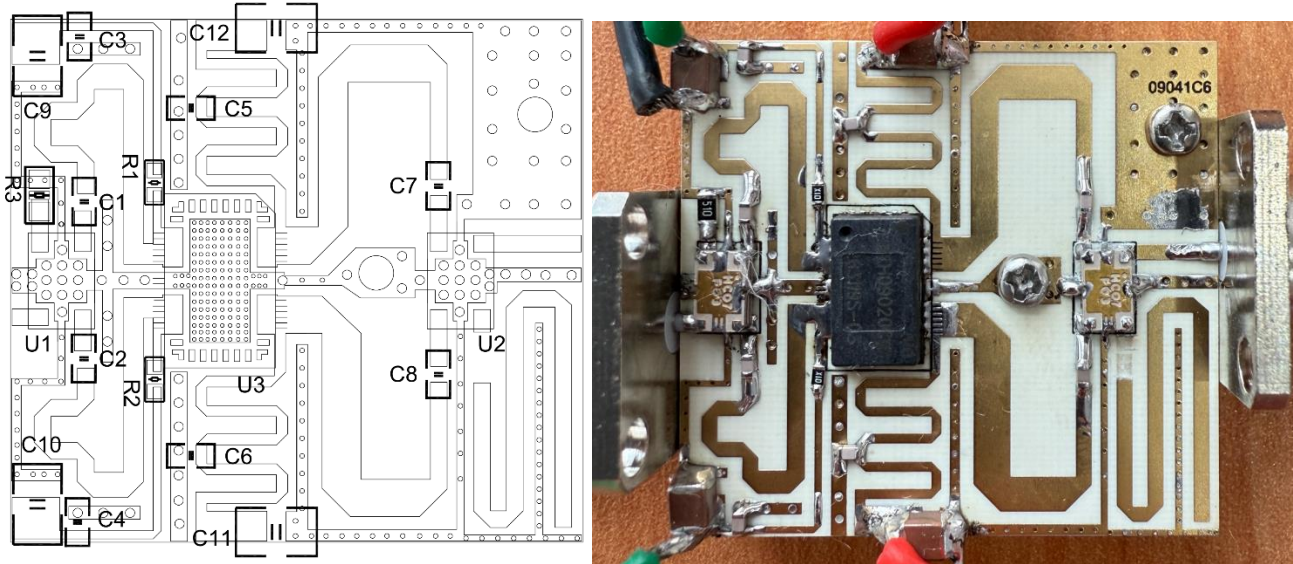


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5, C6, C7	0603	100pF/250V	7
C8	0603	10pF/250V	1
C9, C10, C11, C12	1210	10uF/100V	4
R1, R2	0603	10R	2
R3	0805	10R	1
U1	3.18*5.08mm	HC07F03	2
U2	C6	ITEH09020C6 ^{V0}	1



TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at $I_{dq}=30mA$

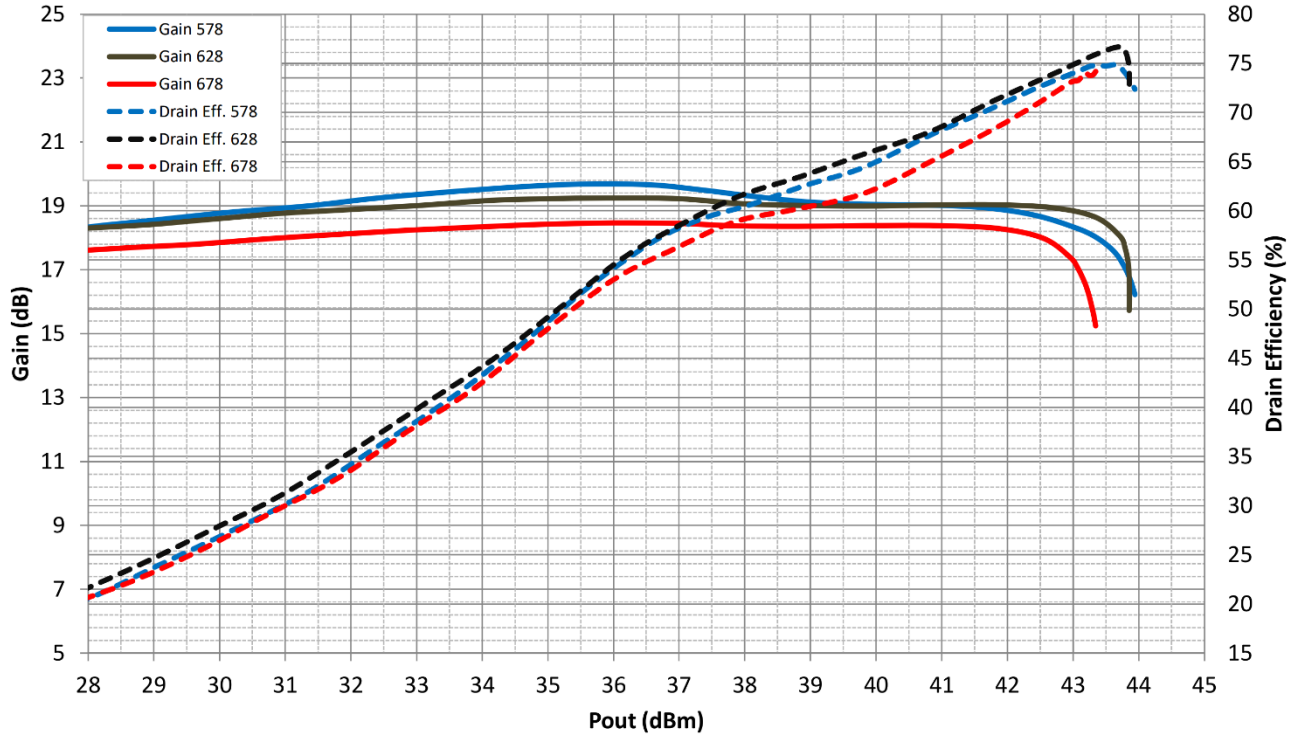
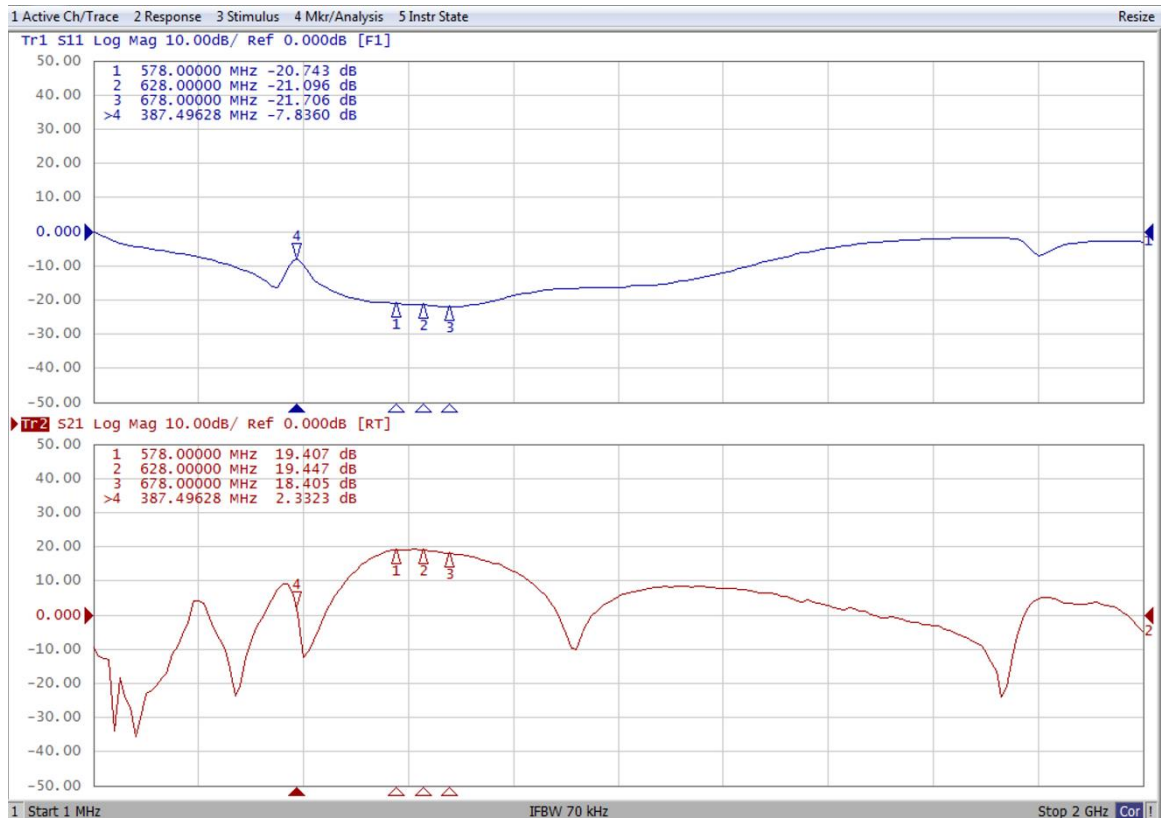


Figure 5. Network analyzer output S11/S21



758-803MHz application board

Reference Circuit of Test Fixture Assembly Diagram

20mils RO4350B

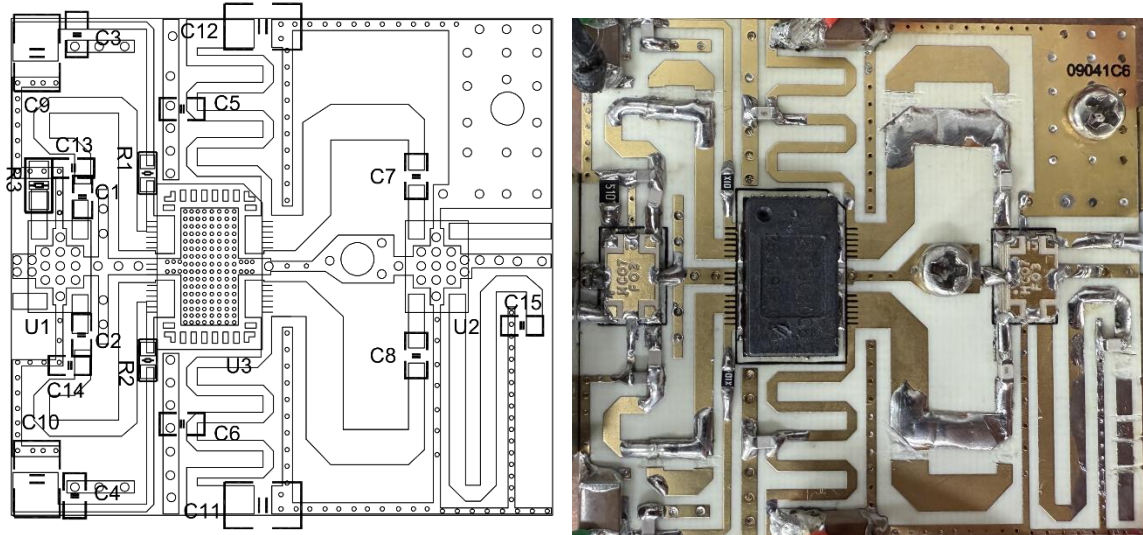


Figure 6. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2	0603	8.2pF/250V	2
C3, C4, C5, C6, C7, C8, C15	0603	68pF/250V	7
C13, C14	0603	3.3pF/250V	2
C9, C10, C11, C12	1210	10uF/100V	4
R1, R2	0603	10R	2
R3	0805	10R	1
U1	3.18*5.08mm	HC07F03	2
U2	C6	ITEH09020C6 ^{V0}	1



TYPICAL CHARACTERISTICS

Figure 7. Power Gain and Drain Efficiency as function of Power Output at Idq=30mA

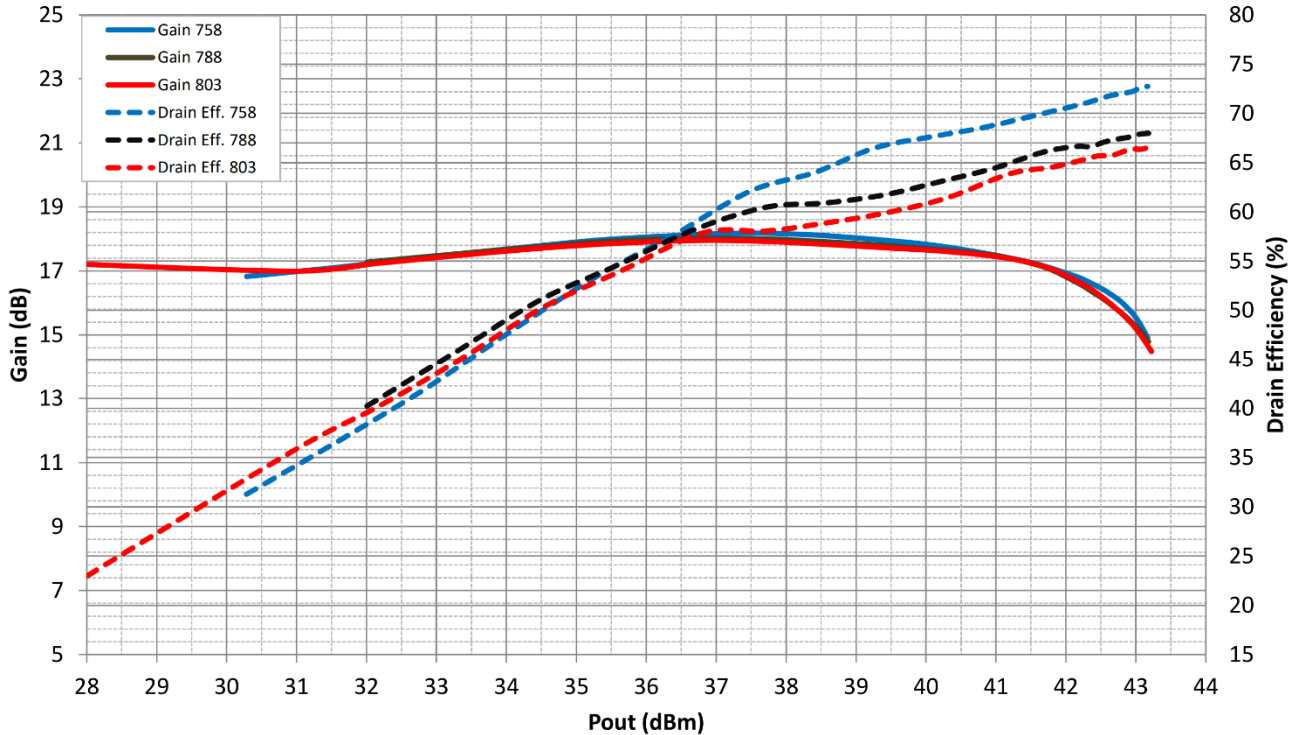
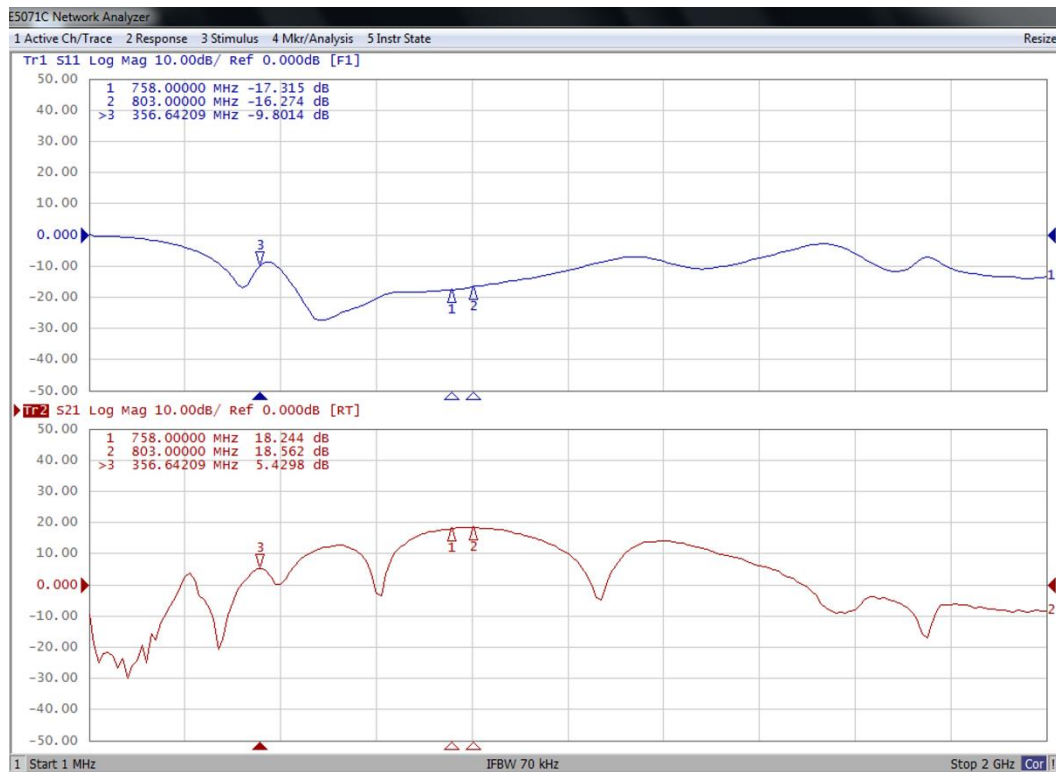
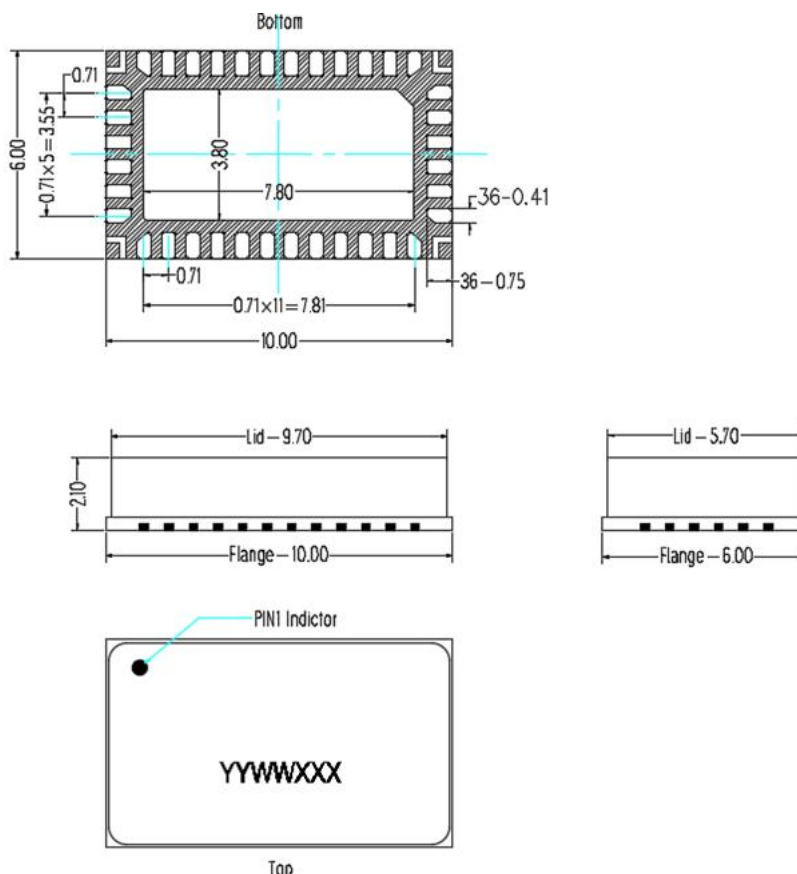


Figure 8. Network analyzer output S11/S21



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are $\pm 0.2\text{mm}$.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2026/8/7	Rev 1.0	Preliminary Datasheet

Application data based on ZBB-26-14/15

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