

150W(75W*2),50V High Power RF LDMOS FETs

ITGV10150C9

Description

The ITGV10150C9 is a dual path 150watt capable, high performance, internally matched LDMOS FET, designed for RF Energy or ISM application centered at 915MHz, in cost effective 12*10mm QFN plastic package.

It can be soldered on PCB through high density grounding vias or soldered directly on heatsink, according to different applications.



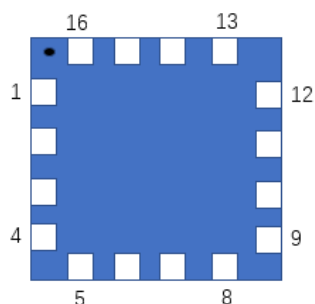
- Typical **single path 75W** CW performance(on Innogration test board with device soldered on heatsink directly)

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
915	48.77	75.4	73.7	18.03	49.01	79.6	73.4

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Pin Configuration and Description (Top view)



Pin No.	Symbol	Description
1,2	RF IN/Vgs1	RF Input/Gate bias of path 1
11,12	RF OUT/Vds1	RF Output/Drain bias of path 1
3,4	RF IN/Vgs2	RF Input/Gate bias of path 2
9,10	RF OUT/Vds2	RF Output/Drain bias of path 2
Others	NC	Can be left as either no use or grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW applications, but will result in excessive junction temperatures and different RF performance

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc

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Preliminary Datasheet V1.0

Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test, soldered on heatsink	R _{θJC}	1.0	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage V _{GS} =0, I _{DS} =1.0mA	V _{(BR)DSS}		110		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 75V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 μA)	V _{GS(th)}	—	2.65	—	V
Gate Quiescent Voltage (V _{DD} =50 V, I _D = 200 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.4	—	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f =915MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 75W Pulsed CW Output Power single path	No Device Degradation
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TYPICAL CHARACTERISTICS of single path

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 915MHz

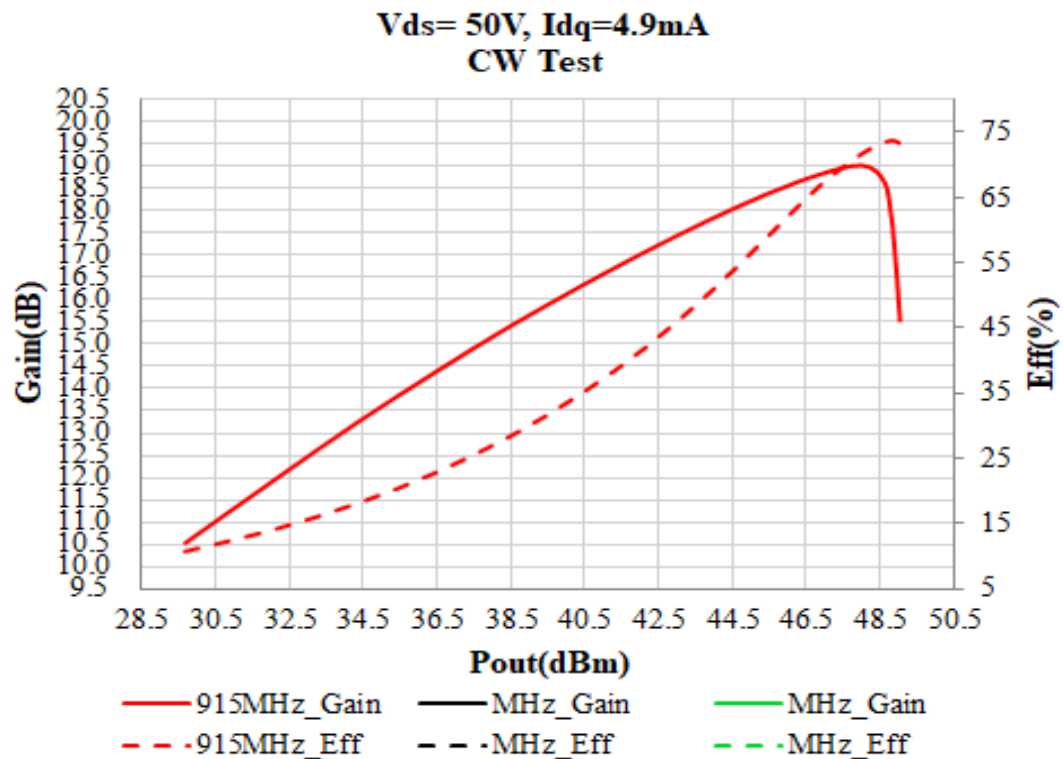
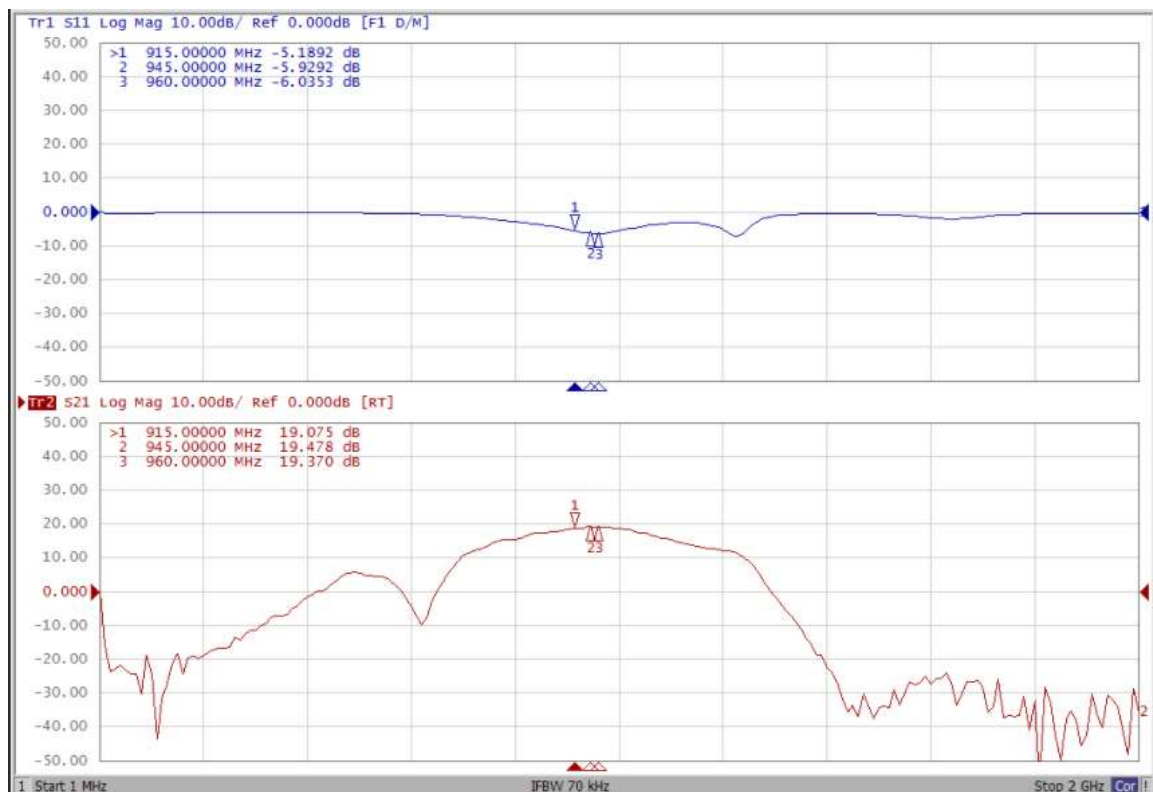


Figure 2: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram

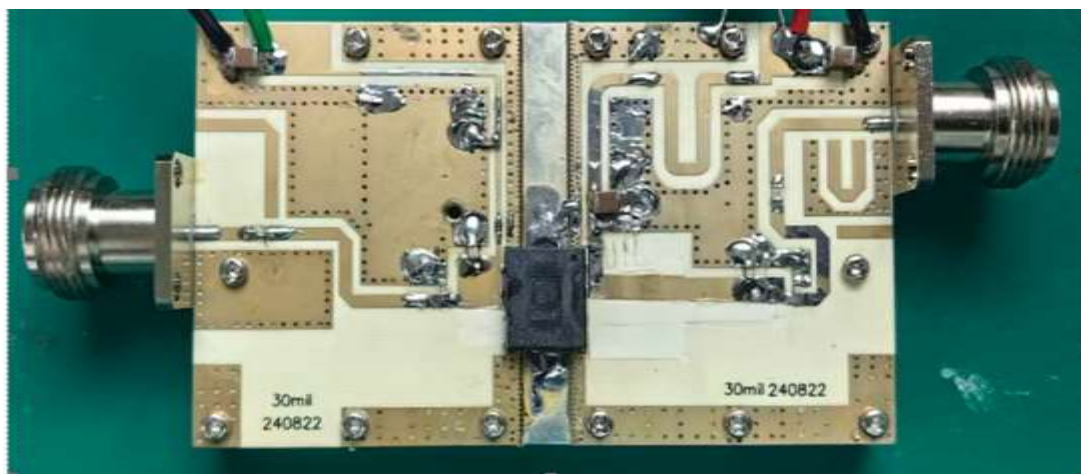
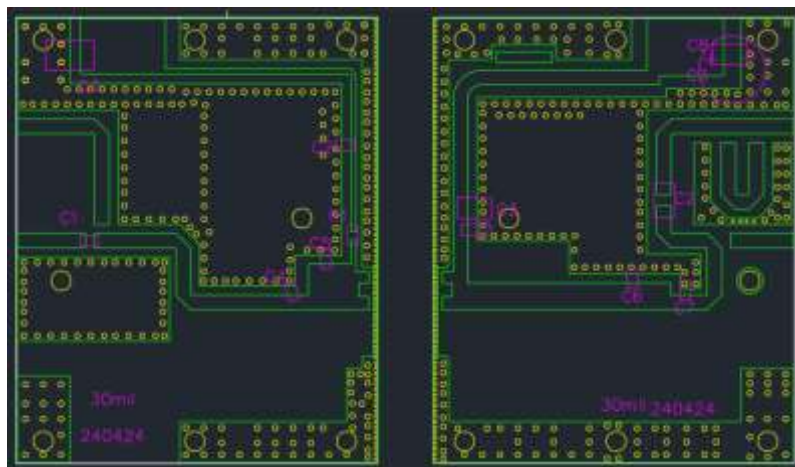
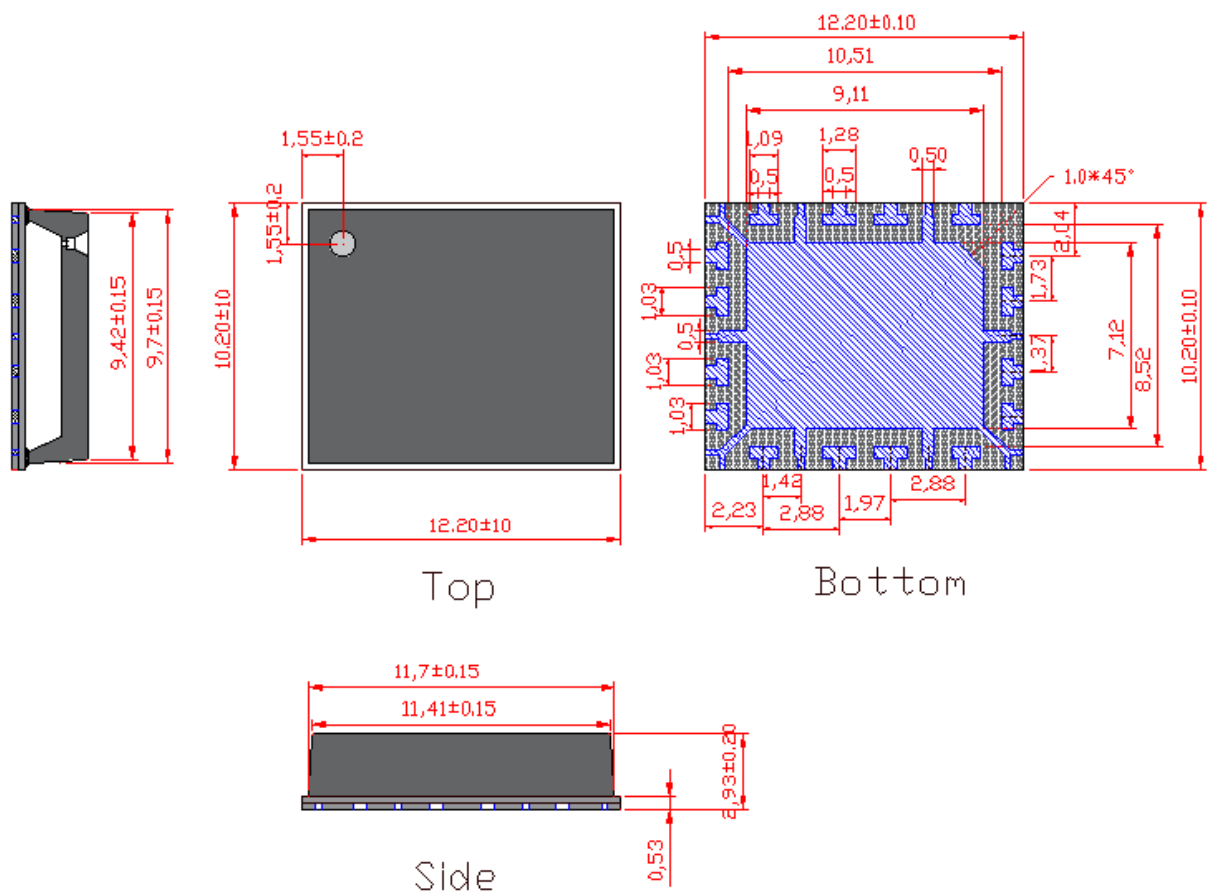


Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
C1	3.9pF	1
C3	10uF	3
R1	10 ohm	1
C2	68pF	3
C4	5.1pF	1
C5	12pF	1
C8	470uF	1
C6	3.9pF	1
C7	2pF	1

Package Dimensions (Unit:mm)



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/9/21	Rev 1.0	Preliminary Datasheet Creation

Application data based on ZYH-26-17

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