



30W,50V 2 stages Matched RF LDMOS Amplifier

I2MGV1822-30

Description

The I2MGV1822-30 is a 30-watt, highly rugged, input fully matched and output partially matched LDMOS FET, designed for multiple applications within 1.8-2.2GHz. It can be used in linear or saturated power amplifier, for modulated and pulsed signal, and any modulation format in highly compact PCB.

It is also featured by its lower cost of plastic open cavity for surface mount on PCB through vias.



- Typical Performance in compact PCB (On Innegration fixture with device soldered).

$V_{ds}=50V$, $V_{gs1}=3.6V$, $I_{dq1}=35mA$, $V_{gs2}=3.3V$, $I_{dq2}=55mA$					
Pulse					
Freq(MHz)	P-1(dBm)	P-1Gain(dB)	P-4(dBm)	P-4(W)	EFF (%)
1800	44.28	28.6	44.79	30.2	44.4
1900	44.42	28.3	45.03	31.8	43.3
2000	44.45	28.6	45.19	33.1	43.9
2100	44.11	29.1	45.14	32.6	43.9
2200	43.12	28.7	44.89	30.8	42.6

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- B1/B3 or N1/N3 narrow band or full band 4G/5G
- E Doherty driver at B1/B3, N1/N3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C=85^{\circ}C$, $T_J=200^{\circ}C$, DC test	$R_{\theta JC}$	1.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2



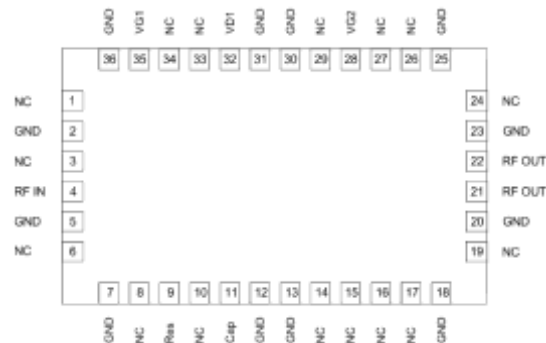
Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0$, $I_{DS}=100\mu A$	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90V$, $V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current of 1 st and 2 nd stage ($V_{GS} = 11V$, $V_{DS} = 0V$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage of 1 st stage ($V_{DS} = 50V$, $I_D = 600\mu A$)	$V_{GS(th)1}$	—	2	—	V
Gate Quiescent Voltage of 1 st stage ($V_{DD} = 50V$, $I_D = 35mA$, Measured in Functional Test)	$V_{GS(Q)1}$	—	3.6	—	V
Gate Threshold Voltage of 2 nd stage ($V_{DS} = 50V$, $I_D = 600\mu A$)	$V_{GS(th)2}$	—	2	—	V
Gate Quiescent Voltage of 2 nd stage ($V_{DD} = 50V$, $I_D = 55mA$, Measured in Functional Test)	$V_{GS(Q)2}$	—	3.3	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 50Vdc$, $I_{DQ1+2} = 100mA$, $f = 2200MHz$

VSWR 10:1 at 30W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Definition (Top View)



Pin No.	Symbol	Description
32	Vds1	Drain voltage 1 st stage
35	Vgs1	Gate voltage 1 st stage
28	Vgs2	Gate voltage 2 nd stage
4	RF in	RF input
21,22	Vds2/RF out	Drain voltage 2 nd stage/RF output
9	Res	Connected with Resistor
11	Cap	Connected with Capacitor
2,5,7,12,13,18,20,23,25,30,31,36	GND	DC/RF Ground
Others	NC	Not connected
Package Base	GND	DC/RF Ground.

Reference Circuit of Test Fixture Assembly Diagram

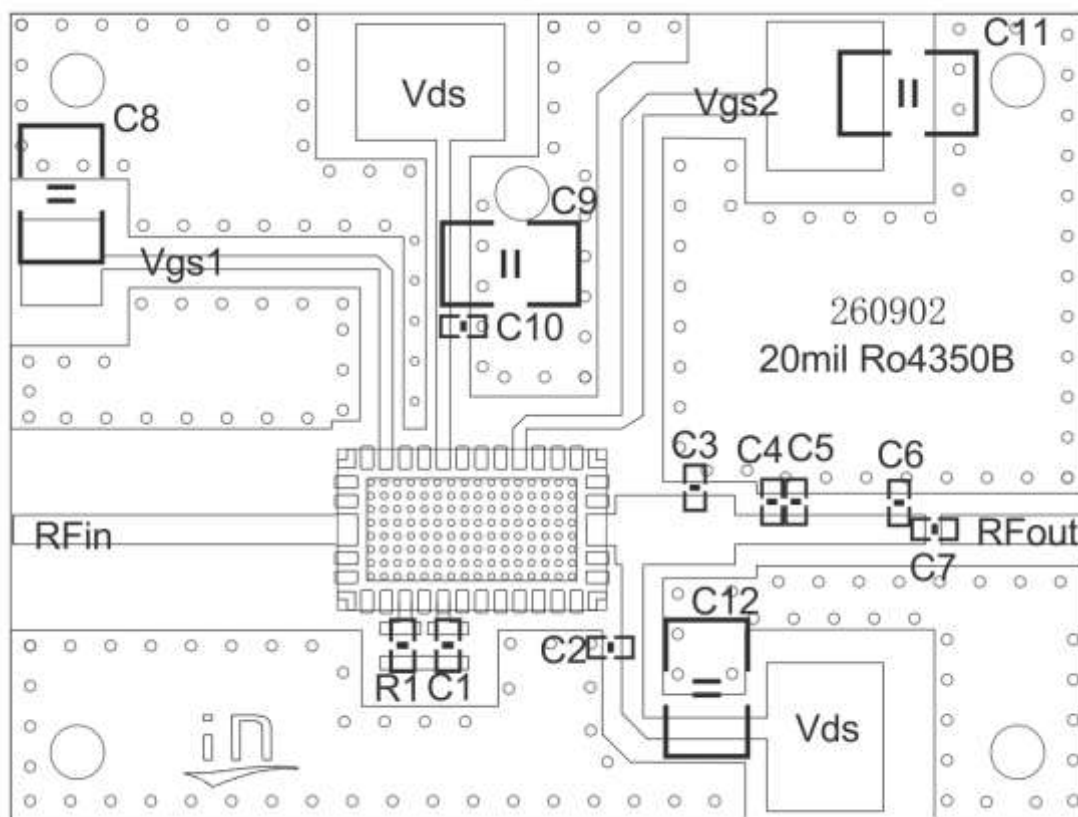


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Value	Description
U1	I2MGV1822-30	PA
C1	0.1pF	0603
C2	10pF	0603
C3	0.5pF	0603
C4、C5、C6	1.2pF	0603
C7	20pF	0603
C8、C9、C11、C12	10uF	1206
C10	1uF	0603
R1	200 Ω	0603

Typical performance

Figure 3: Power gain efficiency as function of Pout

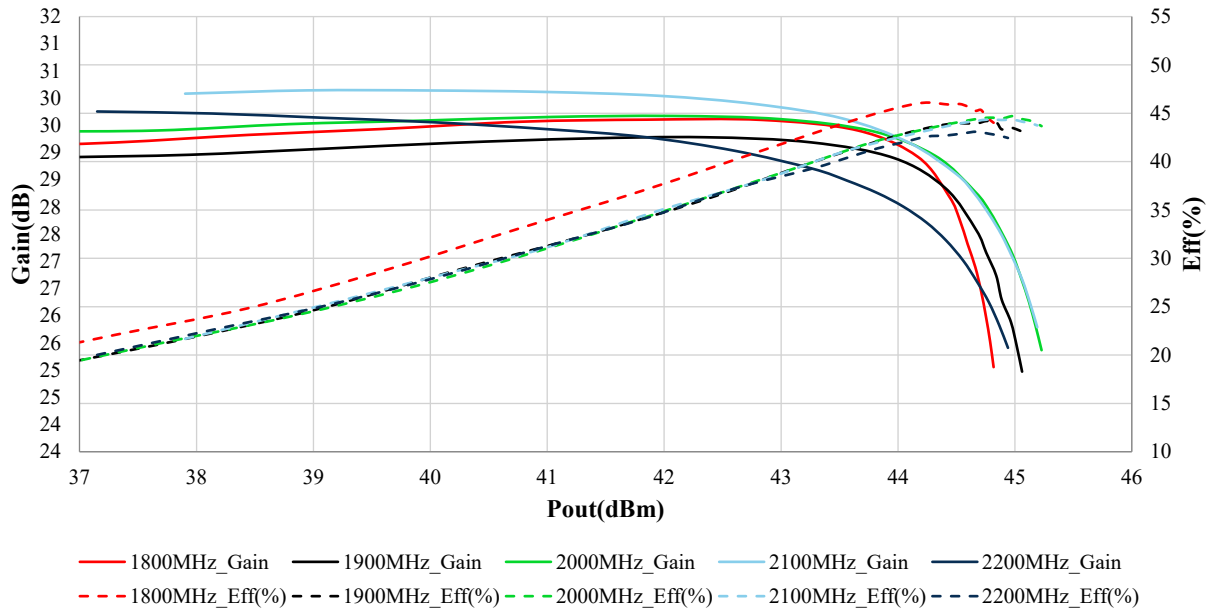
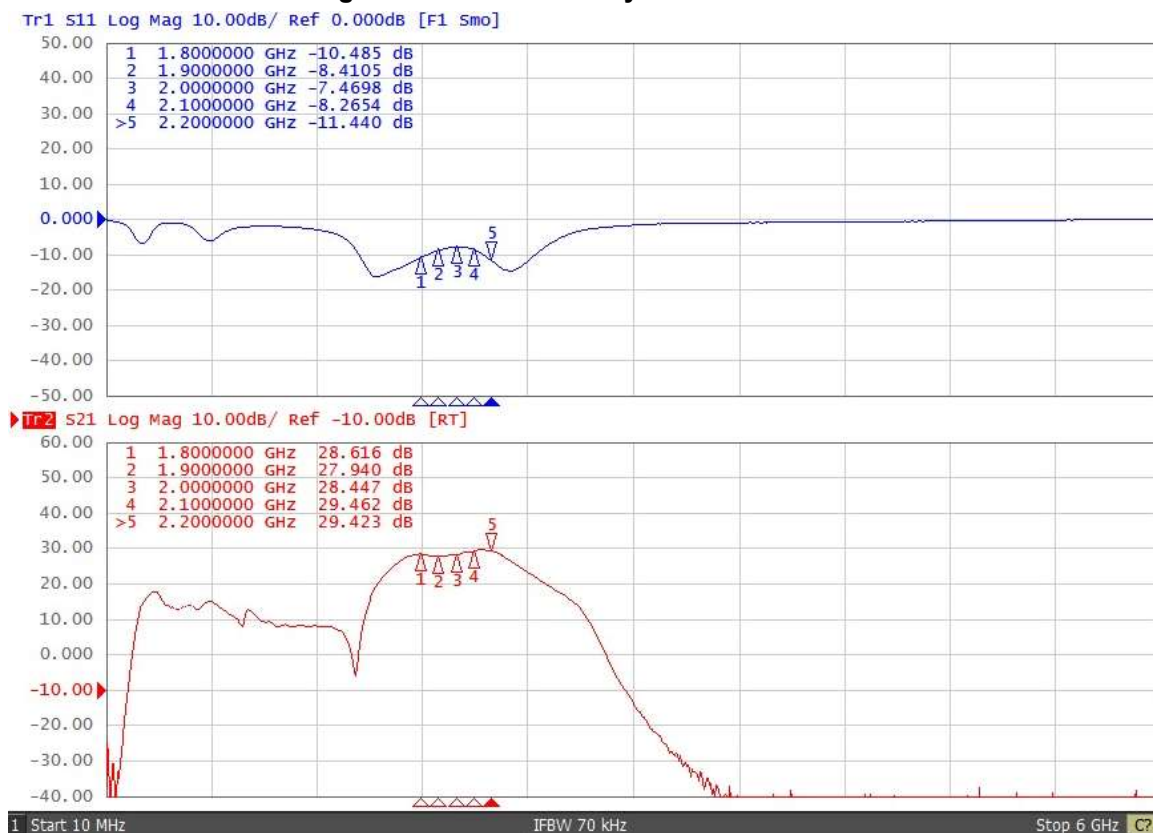


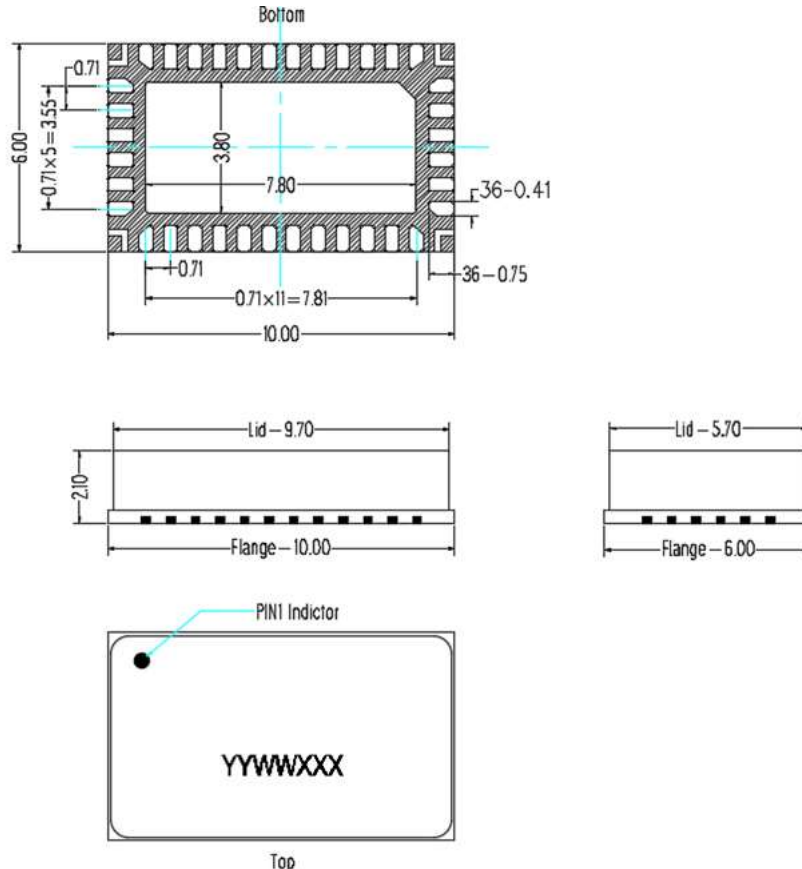
Figure 4: Network analyzer out Pout S11/S21





Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2026/9/28	Rev 1.0	Preliminary Datasheet

Application data based on HJ-26-10

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