

MQ011K7EPX LDMOS TRANSISTOR

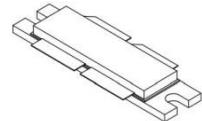
Document Number: MQ011K7EPX
Advanced Datasheet V1.0

1700W, 65V High Power RF LDMOS FETs

Description

The MQ011K7EPX is a 1700W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 250MHz. It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

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Freq(MHz)	Voltage(V)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)	Remark
108	65	Pulsed CW	44	1830	18.3	82	Balun
108	50	CW	42.2	1000	17.8	81	Balun

Features

- High breakdown voltage 190V to enable possible class E operation at lower Vdd up to 50V
- Qualified up to a maximum of VDS = 65 V Class AB
- Characterized from 36 V to 65 V to support a wide range of applications
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCl drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V _{DSS}	190	Vdc
Gate—Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+65	Vdc
Storage Temperature Range	T _{STG}	-65 to +150	°C
Case Operating Temperature	T _C	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case , Case Temperature 85°C, 1700W CW, 65 Vdc, IDQ = 240 mA	R _{θJC}	TBD	°C/W
Transient thermal impedance from junction to case T _j = 150° C; t _p = 100 us; Duty cycle = 20 %	Z _{th}	TBD	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

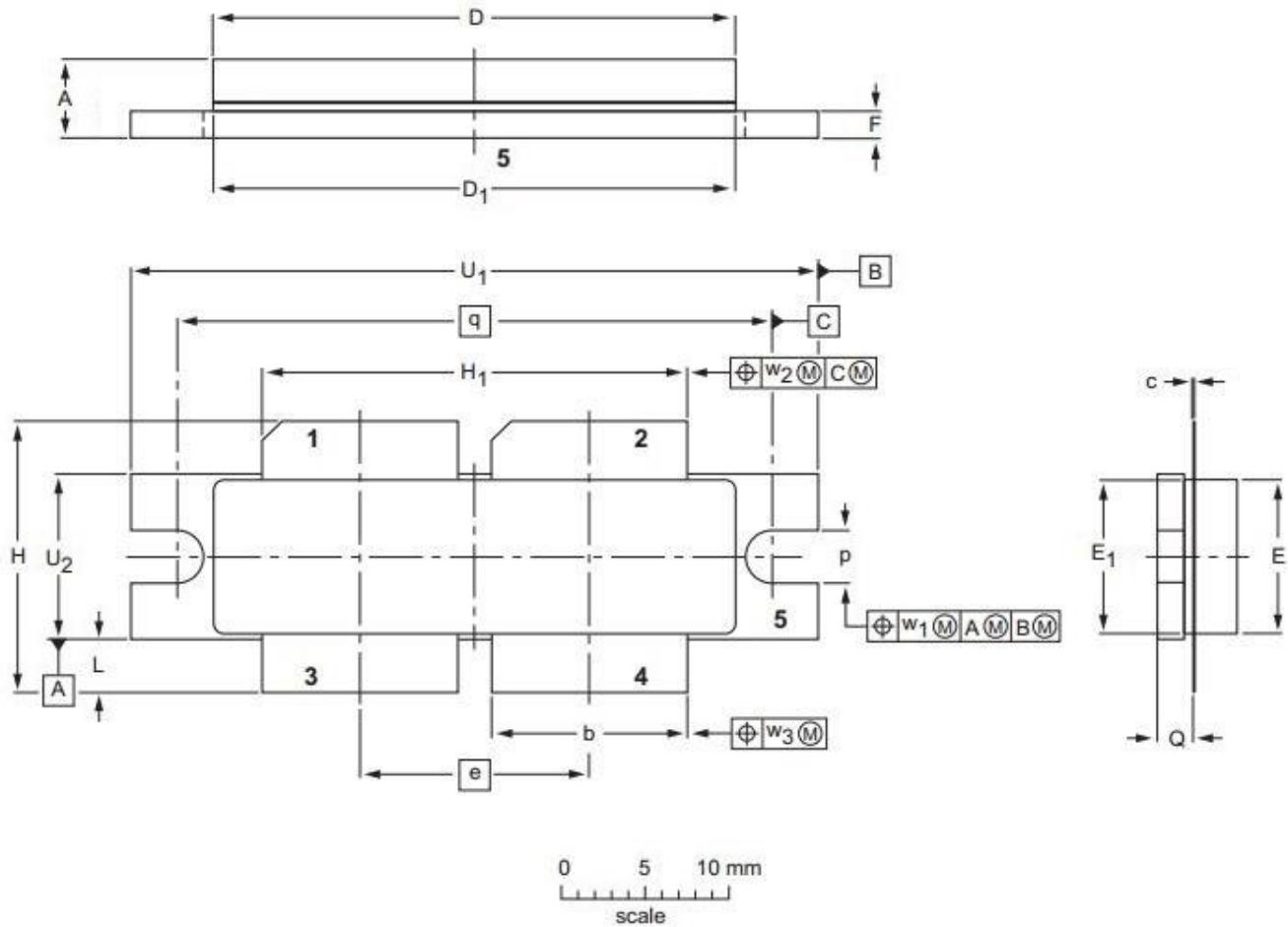
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage (V _{GS} =0V, I _{DS} =20.0 mA)	V _{(BR)DSS}		190		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 55V, V _{GS} = 0 V)	I _{DSS}	—	—	1	µA
Gate—Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	µA
Gate Threshold Voltage (V _{DS} = 55V, I _D = 600 µA)	V _{GS(th)}	—	2.6	—	V
Gate Quiescent Voltage (V _{DD} = 60 V, I _D = 240 mA, Measured in Functional Test)	V _{GS(Q)}	—	3	—	V
Drain source on state resistance (V _{DS} = 0.1V, V _{GS} = 10 V) Each section side of device measured	R _{DS(on)}		125		mΩ
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} = 65 V, f = 1 MHz) Each section side of device measured	C _{ISS}		940		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} = 65 V, f = 1 MHz) Each section side of device measured	C _{OSS}		146		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} = 65 V, f = 1 MHz) Each section side of device measured	C _{RSS}		3.1		pF

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₃
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/12/26	Rev 1.0	Advanced Datasheet

Application data based on HL-25-43

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