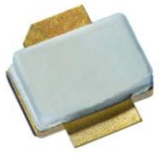
10W,50V Plastic RF LDMOS Transistor

ITGV22010T2



Description

The ITGV22010T2 is a 10-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 2.2GHz, **It is based on air cavity plastic package named as T2 with outline highly compatible as TO270 from other suppliers**

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- RF power amplifiers for CW applications
- Industrial, scientific and medical applications
- Broadcast transmitter applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	5.1	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 90V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V

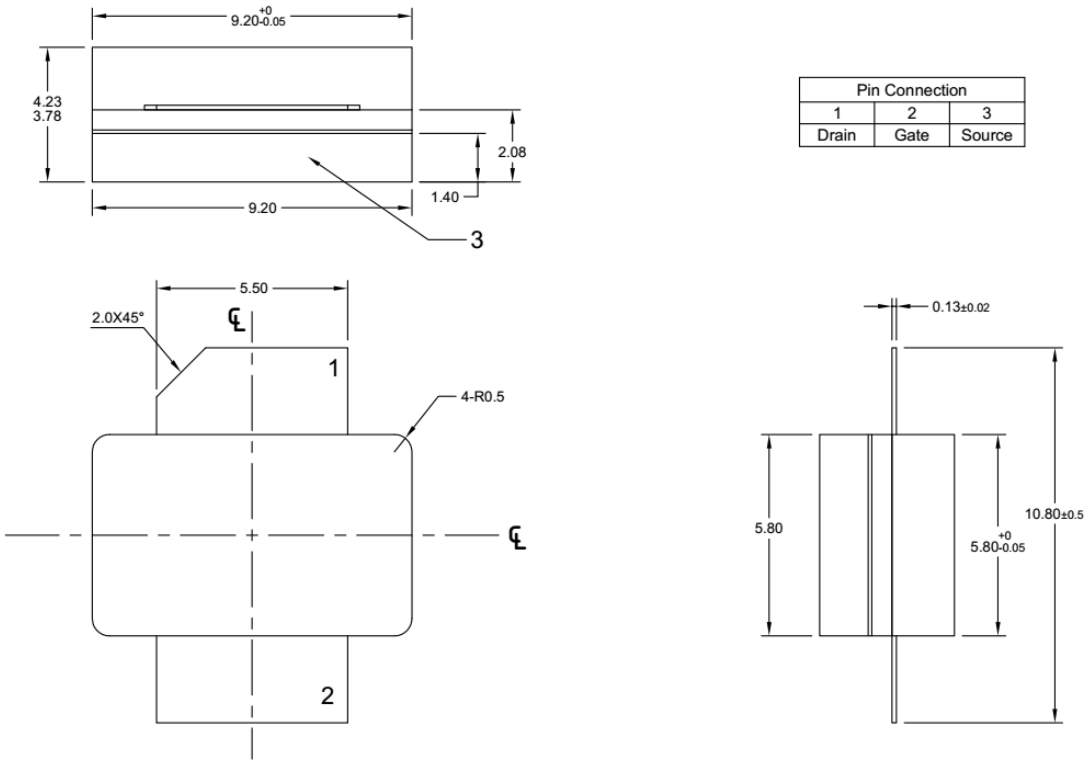
Gate Quiescent Voltage (V_{DD} = 50V, I_D = 25mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.4	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50Vdc, I_{DQ} = 25 mA, f = 2200 MHz

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation

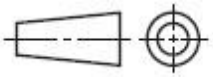
Package Outline

Flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source

Unit：mm
Tolerances(unless specified)：x.x ±0.25
x.xx ±0.13

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-T2/G2C					2018.1.31

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/12/30	Rev 1.0	Preliminary Datasheet

Application data based on

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