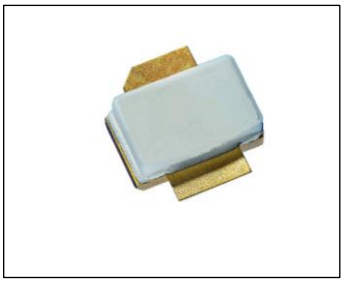
100W,28V Sub-1.5GHz RF LDMOS Transistor



Description

The ITGH15100T2 is a 100-watt, high performance, LDMOS transistor, designed for any general applications at frequencies up to 1.5GHz. **It is based on air cavity plastic package named as T2 with outline highly compatible as TO270 from other suppliers**

- Typical 915MHz Class AB RF Performance (On Innogration fixture with device soldered).

Vds=28V,Idq=200mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1400	49.44	88.0	63.0	15.38	50.22	105.2	65.1

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- RF power amplifiers for CW applications
- Industrial, scientific and medical applications
- Broadcast transmitter applications
-

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, DC test, **device soldered on heatsink directly**	RθJC	0.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	——	——	1	μA

(V_{DS} = 28V, V_{GS} = 0 V)					
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_D = 400mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.5	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 200 mA, f = 915 MHz

VSWR 10:1 at 100W pulse CW Output Power	No Device Degradation

1400MHz application board

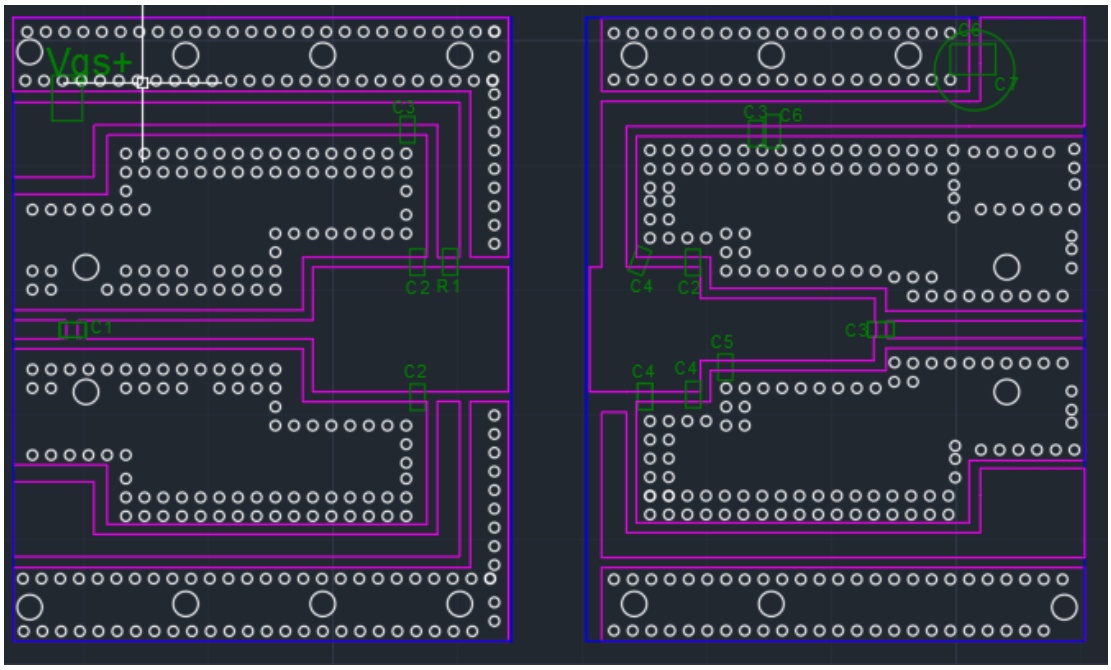


Figure 2. Test Circuit Component Layout, 30mils RO4350B

Note:

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
C3	30pF	3
C1	3.9pF	1
R1	10 ohm	1
C6	10uF	4
C7	470uF	1
C4	0.5pF	3
C2	4.7pF	3
C5	1.8pF	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output

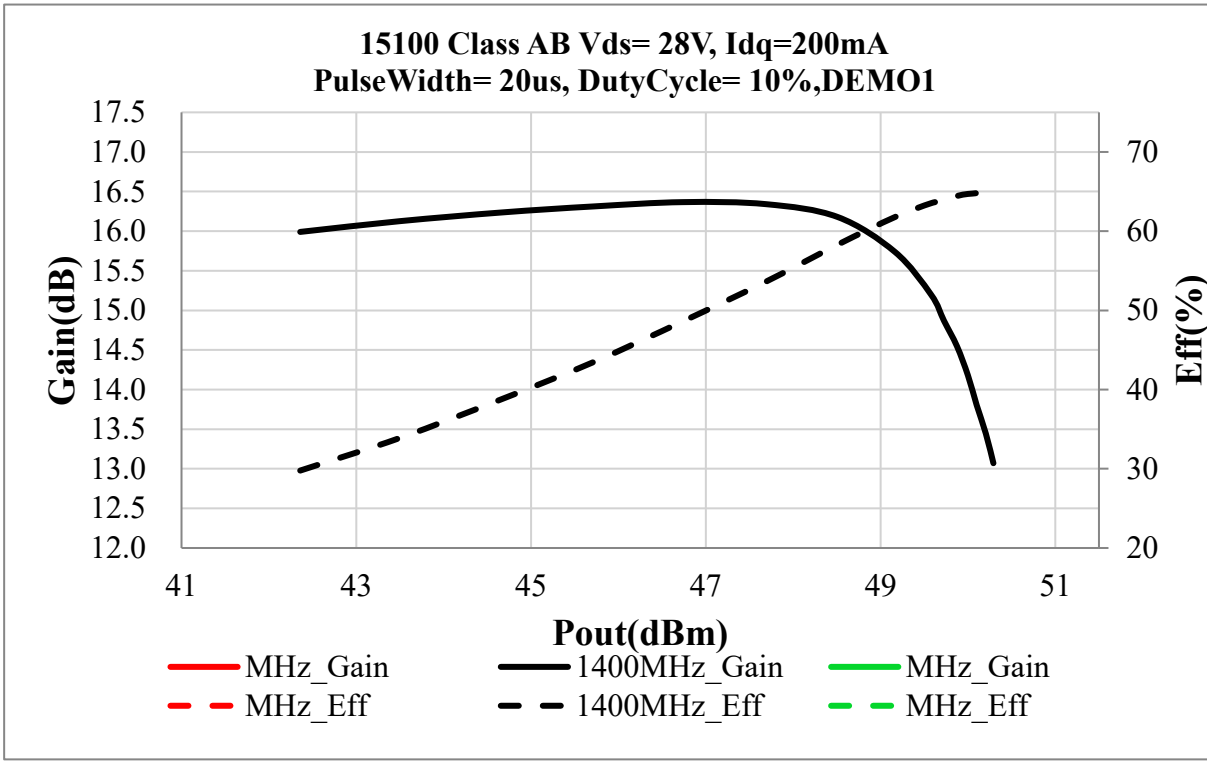
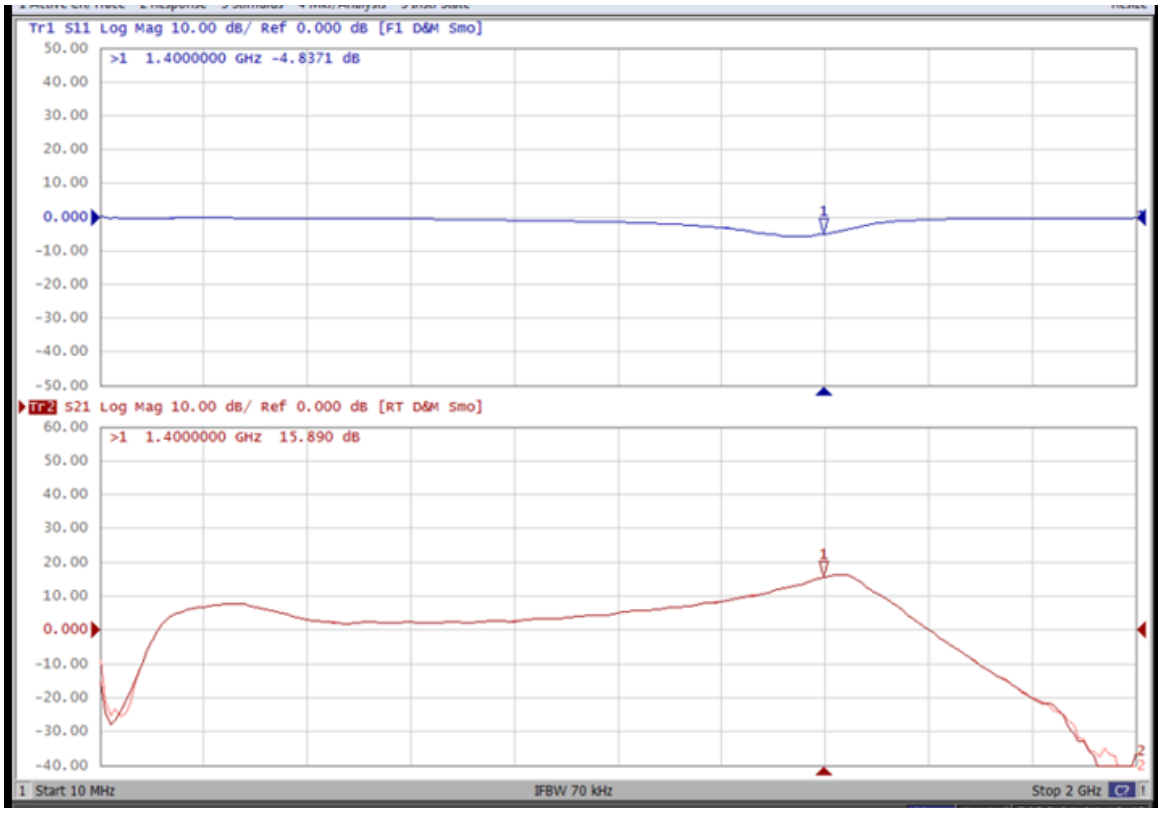
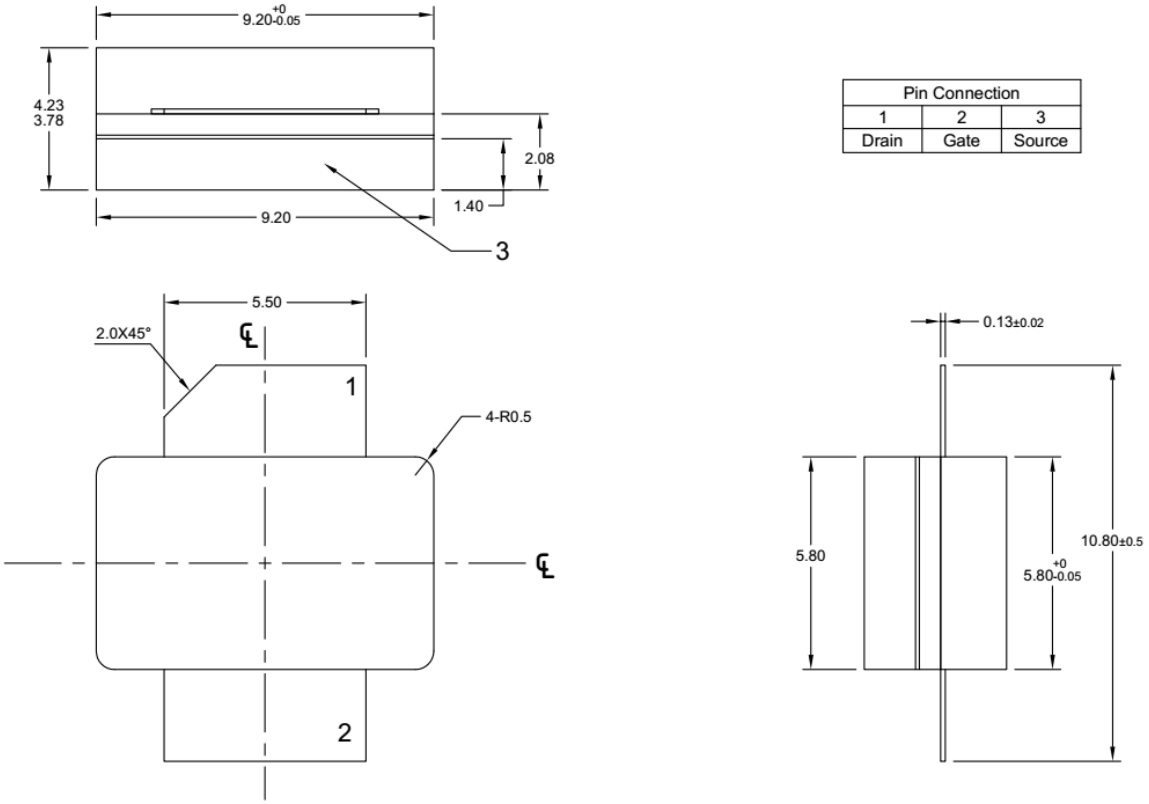


Figure 4. Network analyzer output S11/S21



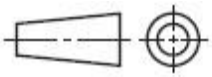
Package Outline

Flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.25
x.xx ±0.13

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-T2/G2C					2018.1.31

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2026/1/4	Rev 1.0	Preliminary Datasheet

Application data based on ZXY-26-01

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