MQ013K0EPX LDMOS TRANSISTOR

Document Number: MQ013K0EPX
Advanced Datasheet V1.0

3000W, 65V High Power RF LDMOS FETs

MQ013K0EPX

Description

The MQ013K0EPX is a 3000W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 250MHz.

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

Please notice that due to internal configuration of both input and output leads, dual path of this device must be configured as in-phase combination, NOT 180dgree Balun or 90 degree hybrid combination.

Freq(MHz)	Voltage(V)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)	Remark
13.56	65	Pulsed CW	45	3300	20	75	In phase combiner
13.56	50	CW	45	1900	19	75	In phase combiner

Features

- High breakdown voltage 190V to enable possible class E operation at lower Vdd up to 50V
- Qualified up to a maximum of VDS = 65 V Class AB
- Characterized from 36 V to 65 V to support a wide range of applications
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	190	Vdc
Gate—Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+65	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 2000W CW, 65 Vdc, I_{DQ} = 240 mA	$R_{\theta JC}$	TBD	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	TBD	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

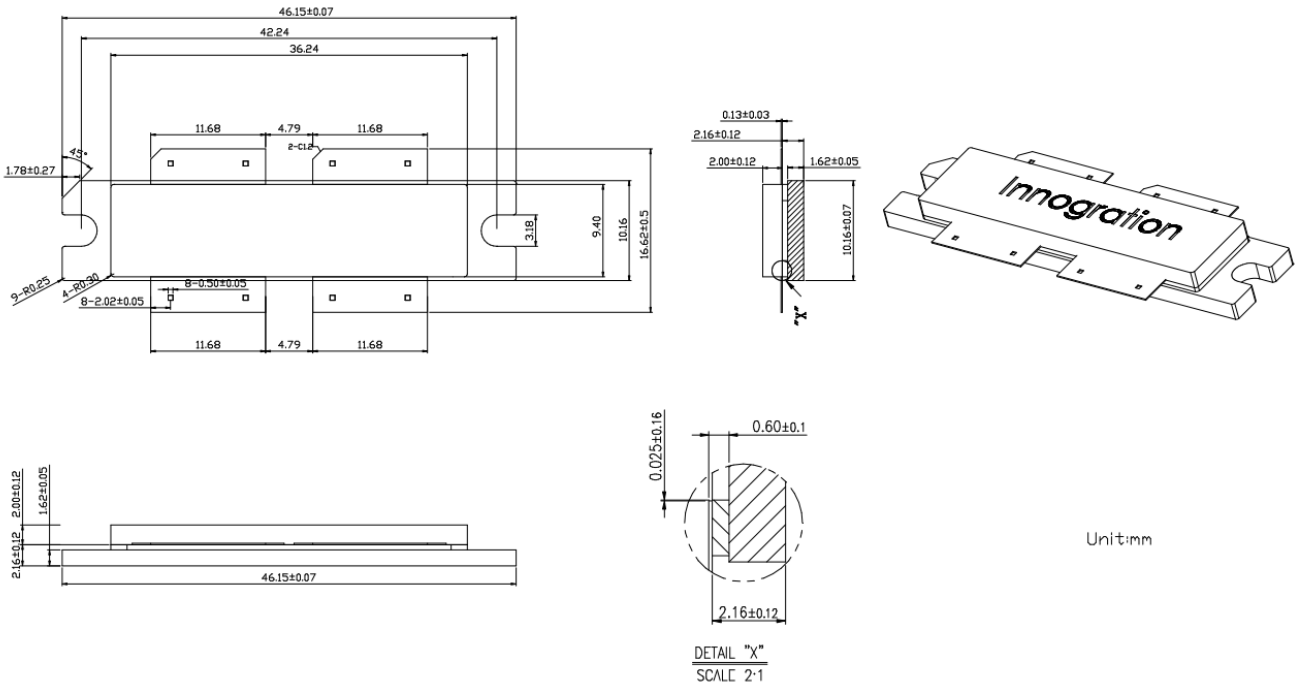
Human Body Model (per JESD22—A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=20.0mA	$V_{(BR)DSS}$		190		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 65V, I_D = 600 μA)	$V_{GS(th)}$	——	2.6	——	V
Gate Quiescent Voltage (V_{DD} = 65 V, I_D = 240 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		85		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =65 V, f = 1 MHz) Each section side of device measured	C_{ISS}		1700		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =65 V, f = 1 MHz) Each section side of device measured	C_{OSS}		250		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =65 V, f = 1 MHz) Each section side of device measured	C_{RSS}		5.5		pF

Package Outline

Flanged ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-O4E					**5/6/2024**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/1/9	Rev 1.0	Advanced Datasheet

Application data based on HL-26-01

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