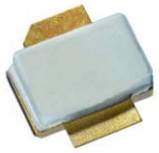
170W,50V Plastic RF LDMOS Transistor

ITEV10170T2



Description

The ITEV10170T2 is a 170-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 1GHz. **It is based on air cavity plastic package named as T2 with outline highly compatible as TO270 from other suppliers**

- Typical Class AB RF Performance (On Innogration fixture with device soldered).

Vds=50V, Idq=50mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
700	51.39	137.9	72.0	22.15	52.38	172.9	73.5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- RF power amplifiers for CW applications
- Industrial, scientific and medical applications
- Broadcast transmitter applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 90V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA

Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 50V, I_D = 300mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50Vdc, I_{DQ} = 300mA, f = 1000 MHz

VSWR 10:1 at 170W pulse CW Output Power	No Device Degradation

700MHz application board

Reference Circuit of Test Fixture Assembly Diagram
30mils RO4350B

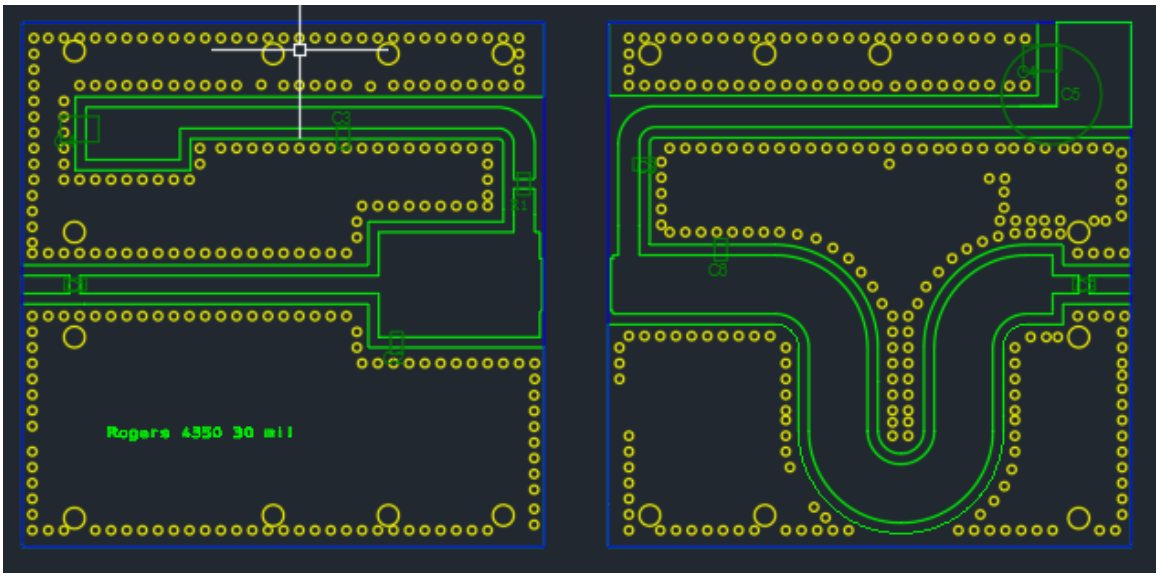


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
C3	30pF	3
C1	3.9pF	1
R1	10 ohm	1
C4	10uF	2
C5	470uF	1
C2	22pF	1
C6	20pF	1

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output)

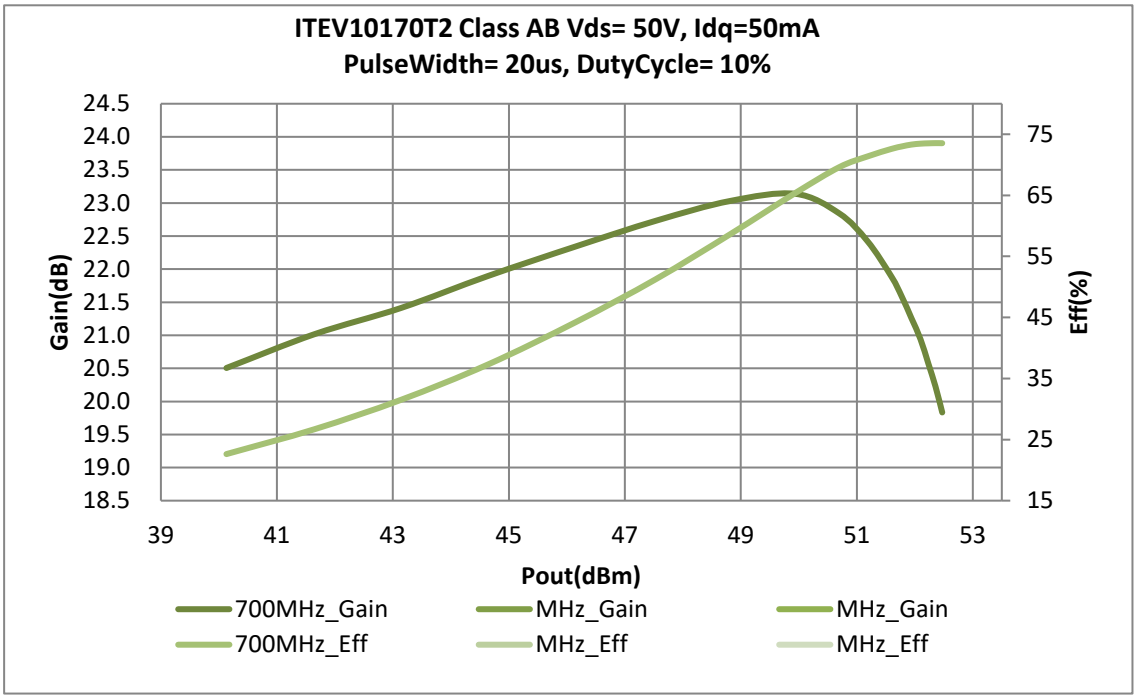
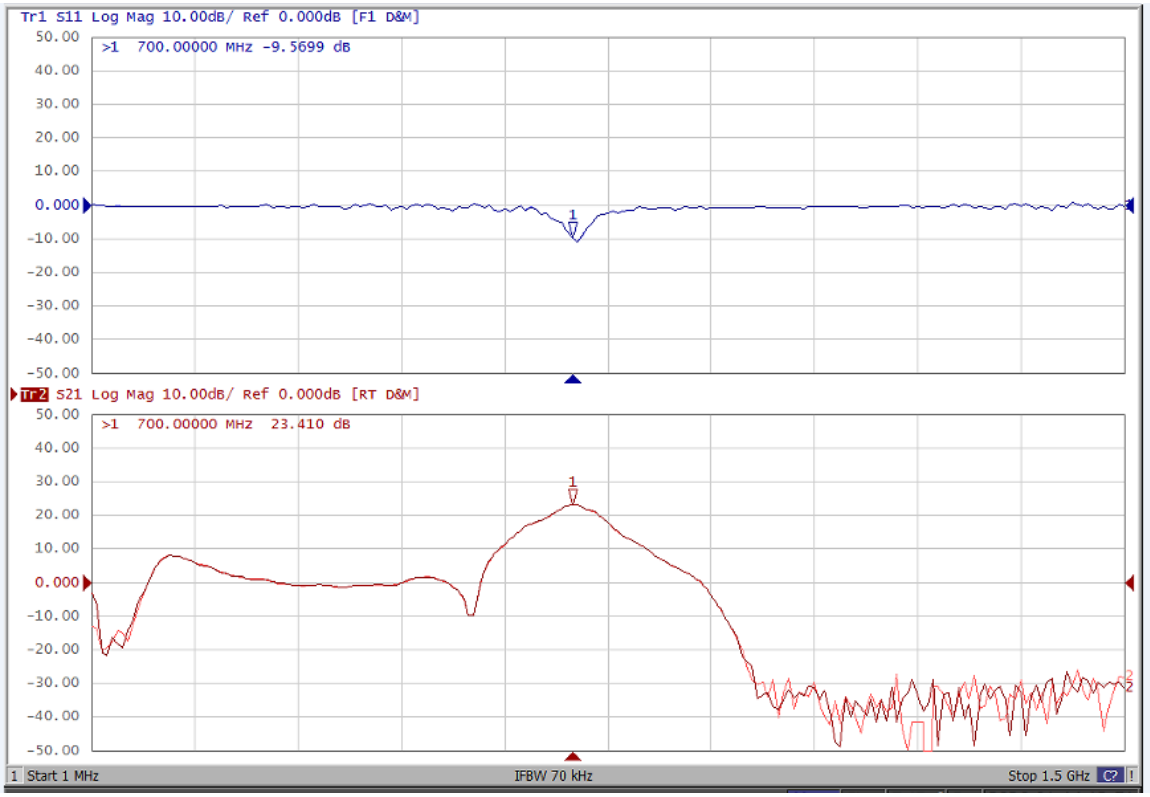
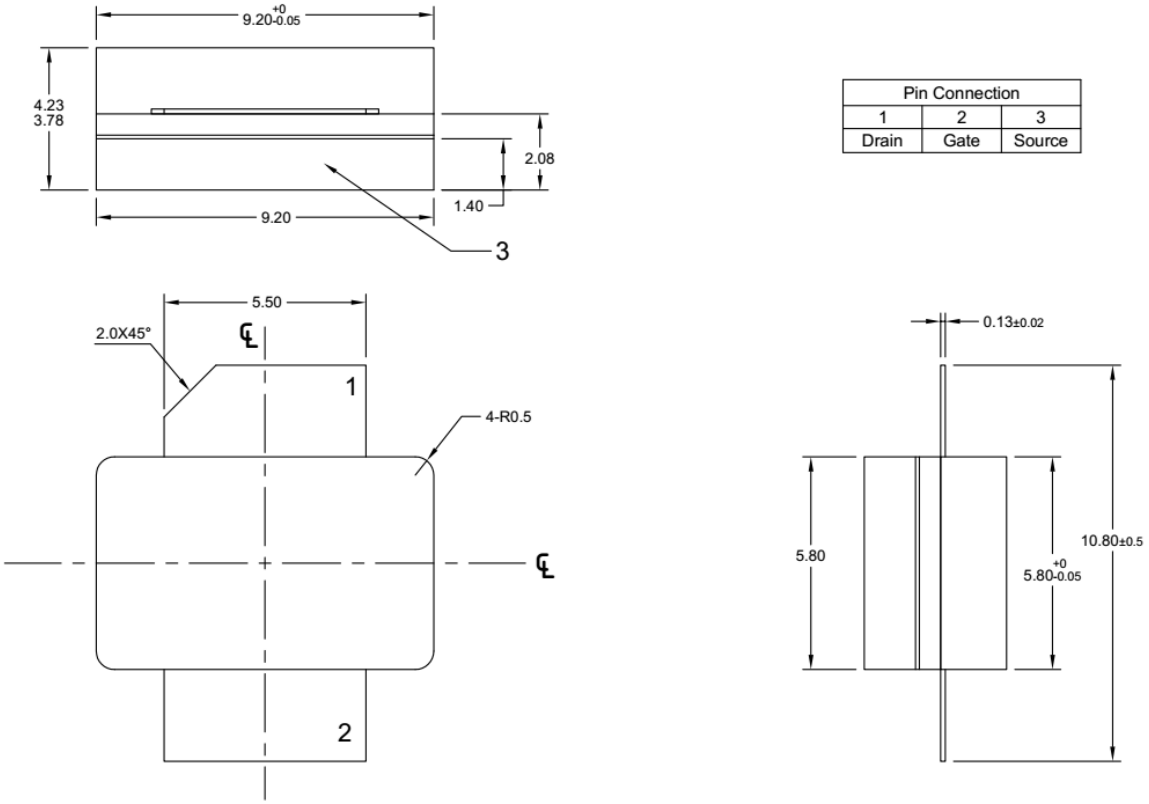


Figure 5.Network analyzer output S11/S21



Package Outline

Flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.25
x.xx ±0.13

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-T2/G2C					2018.1.31

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2026/1/14	Rev 1.0	Preliminary Datasheet

Application data based on ZXY-26-02

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