



## 100W,28V Sub-1.5GHz RF LDMOS Transistor

### Description

The ITGH15100T2C is a 100-watt, high performance, LDMOS transistor, designed for any general applications at frequencies up to 1.5GHz. **It is based on air cavity plastic package named as T2C with outline highly compatible as TO270 from other suppliers**



- Typical 915MHz Class AB RF Performance (On Innegration fixture with device soldered).

**V<sub>ds</sub>=28V, I<sub>dq</sub>=200mA**

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
1400	49.44	88.0	63.0	15.38	50.22	105.2	65.1

### Features

- High Efficiency and Linear Gain Operations
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Pb-free, RoHS-compliant

### Suitable Applications

- RF power amplifiers for CW applications
- Industrial, scientific and medical applications
- Broadcast transmitter applications
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**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+65	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+28	Vdc
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T <sub>j</sub>	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T <sub>c</sub> = 85°C, DC test, <b>device soldered on heatsink directly</b>	R <sub>θJC</sub>	0.6	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### DC Characteristics

Drain-Source Voltage V <sub>GS</sub> =0, I <sub>DS</sub> =100uA	V <sub>(BR)DSS</sub>		65		V
Zero Gate Voltage Drain Leakage Current	I <sub>loss</sub>	—	—	1	μA



( $V_{DS} = 28V, V_{GS} = 0V$ )					
Gate--Source Leakage Current ( $V_{GS} = 11V, V_{DS} = 0V$ )	$I_{GSS}$	—	—	1	$\mu A$
Gate Threshold Voltage ( $V_{DS} = 28V, I_D = 600\mu A$ )	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ( $V_{DD} = 28V, I_D = 400mA$ , Measured in Functional Test)	$V_{GS(Q)}$	—	2.5	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system):  $V_{DD} = 28Vdc, I_{DQ} = 200mA, f = 915MHz$

VSWR 10:1 at 100W pulse CW Output Power	No Device Degradation
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### 1400MHz application board

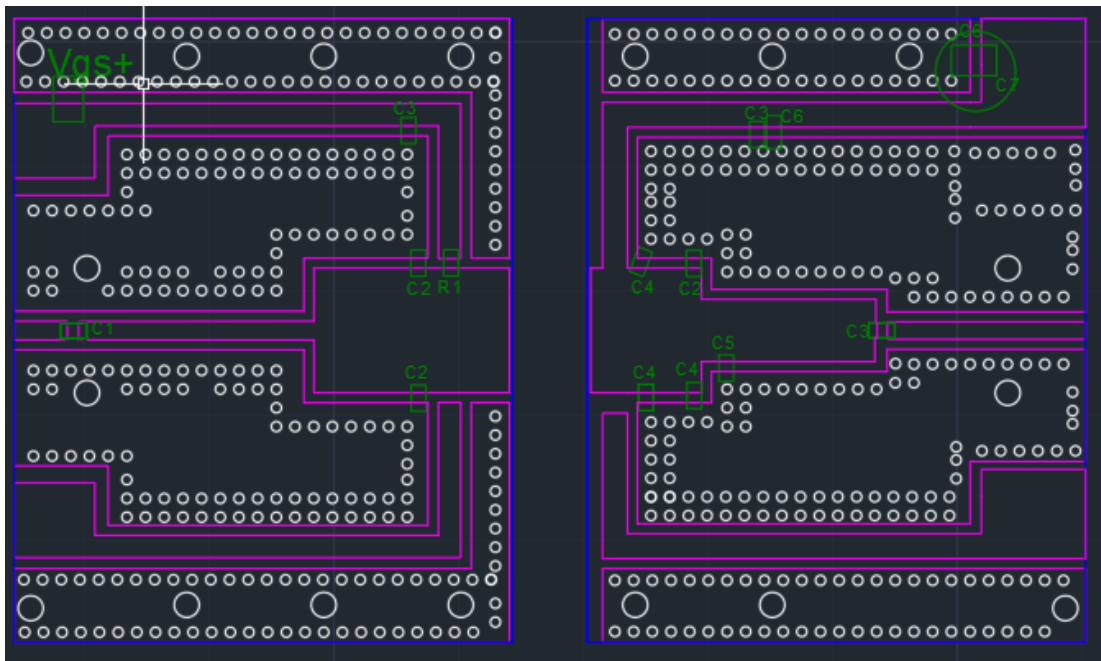


Figure 2. Test Circuit Component Layout, 30mils RO4350B

Note:

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
C3	30pF	3
C1	3.9pF	1
R1	10 ohm	1
C6	10uF	4
C7	470uF	1
C4	0.5pF	3
C2	4.7pF	3
C5	1.8pF	1



### TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output

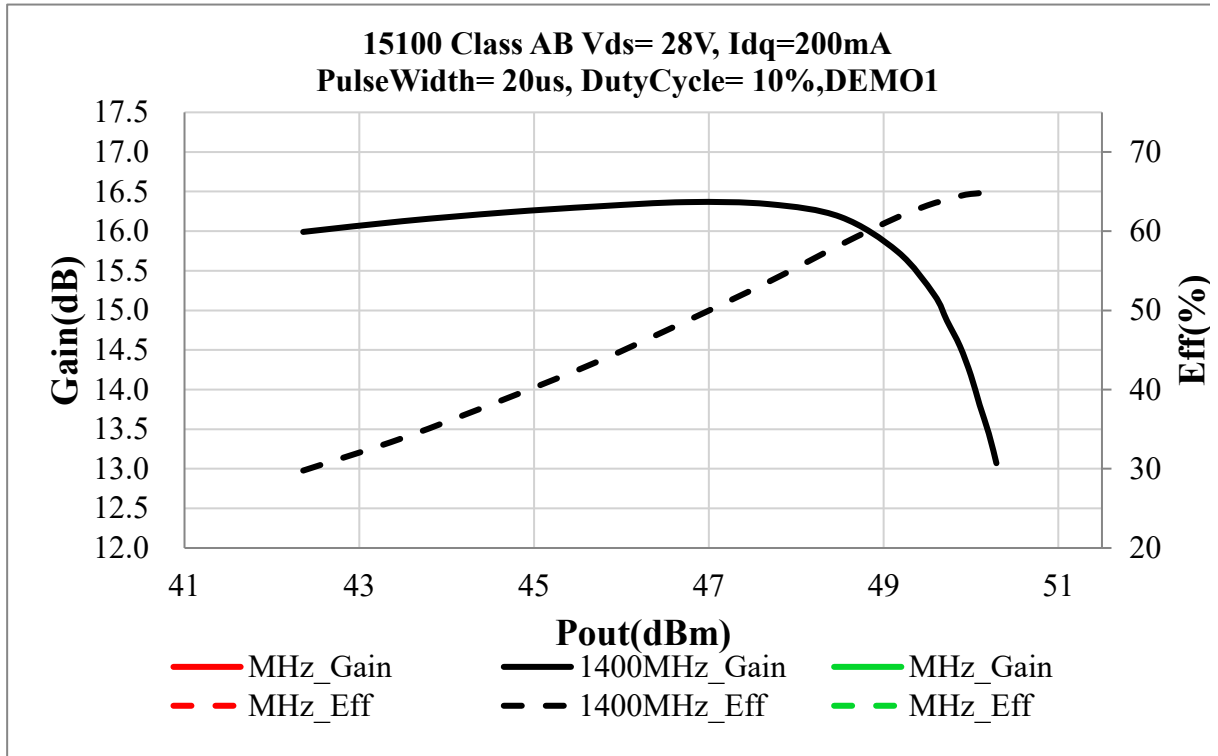
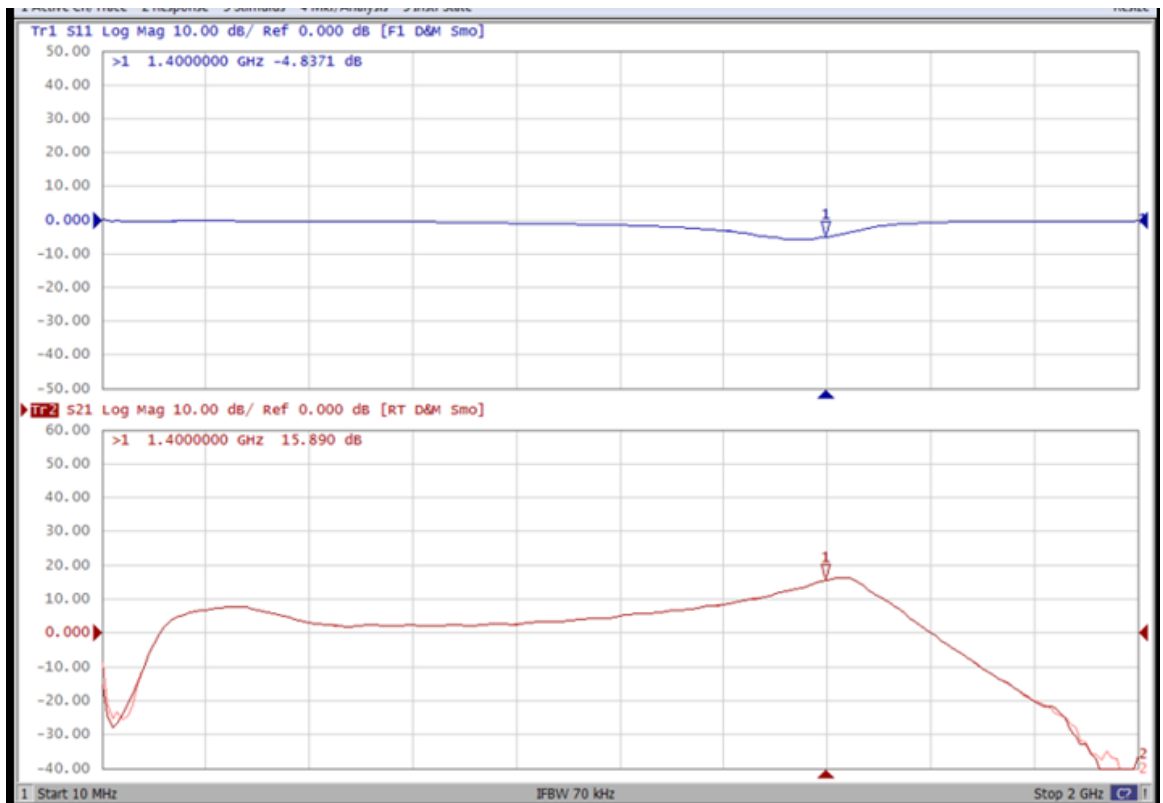


Figure 4. Network analyzer output S11/S21



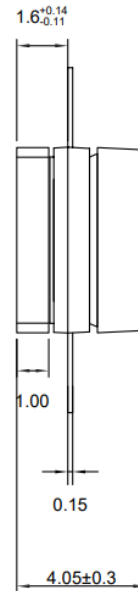
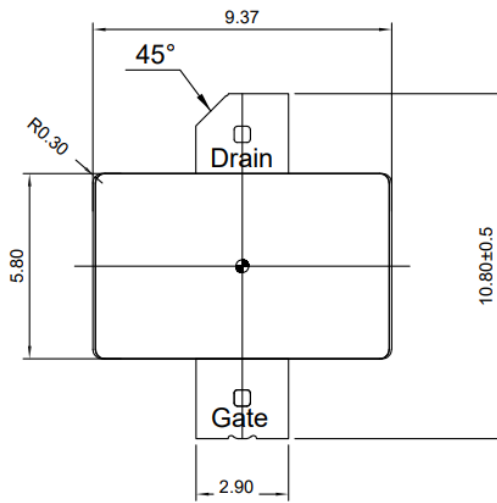
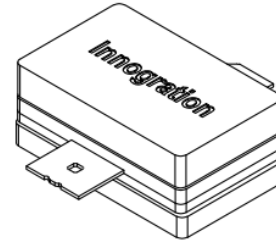
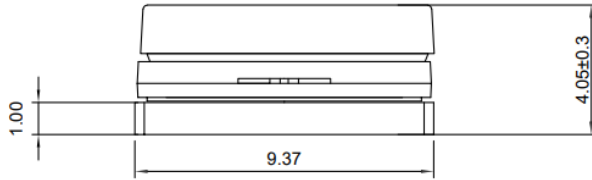


## Package Outline

Flanged ceramic package; 2 leads

# T2C POD

Rev.01 (2026.01.20)



Unit:mm  
Tolerances(unless specified): x.x ±0.1

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-T2C					2018.1.31



## Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2026/1/4	Rev 1.0	Preliminary Datasheet

Application data based on ZXY-26-01

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