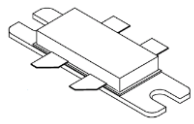
MK0170EPX LDMOS TRANSISTOR

Document Number: MK0170EPX
Advanced Datasheet V1.0

700W/400W, 65V/50V High Power RF LDMOS FETs

MK0170EPX



Description

The MK0170EPX is a 700W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 250MHz.

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

Freq(MHz)	Voltage(V)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)	Harmonic $2^{nd}/3^{rd}$ (dBc)
108	65	CW	38.5	710	20	82	-30/-40

Features

- High breakdown voltage 190V to enable possible class E operation at lower Vdd up to 50V
- Qualified up to a maximum of VDS = 65 V Class AB
- Characterized from 36 V to 65 V to support a wide range of applications
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	190	Vdc
Gate—Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+65	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 700W CW, 65 Vdc, I_{DQ} = 240 mA	$R_{\theta JC}$	TBD	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	TBD	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					

Drain-Source Voltage V_{GS}=0V, I_{DS}=20.0 mA	$V_{(BR)DSS}$		190		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 55V, I_D = 600 μA)	$V_{GS(th)}$	——	2.6	——	V
Gate Quiescent Voltage (V_{DD} = 60 V, I_D = 240 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		250		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =65 V, f = 1 MHz) Each section side of device measured	C_{ISS}		470		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =65 V, f = 1 MHz) Each section side of device measured	C_{OSS}		74		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =65 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.6		pF

108MHz

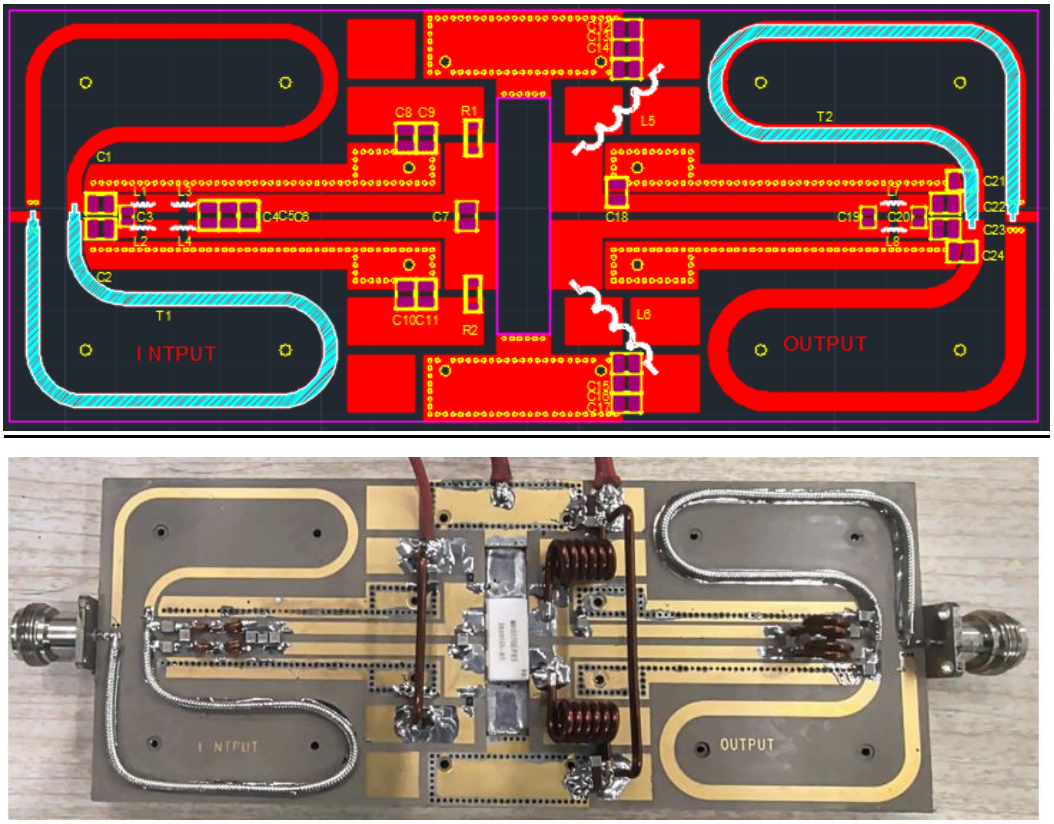
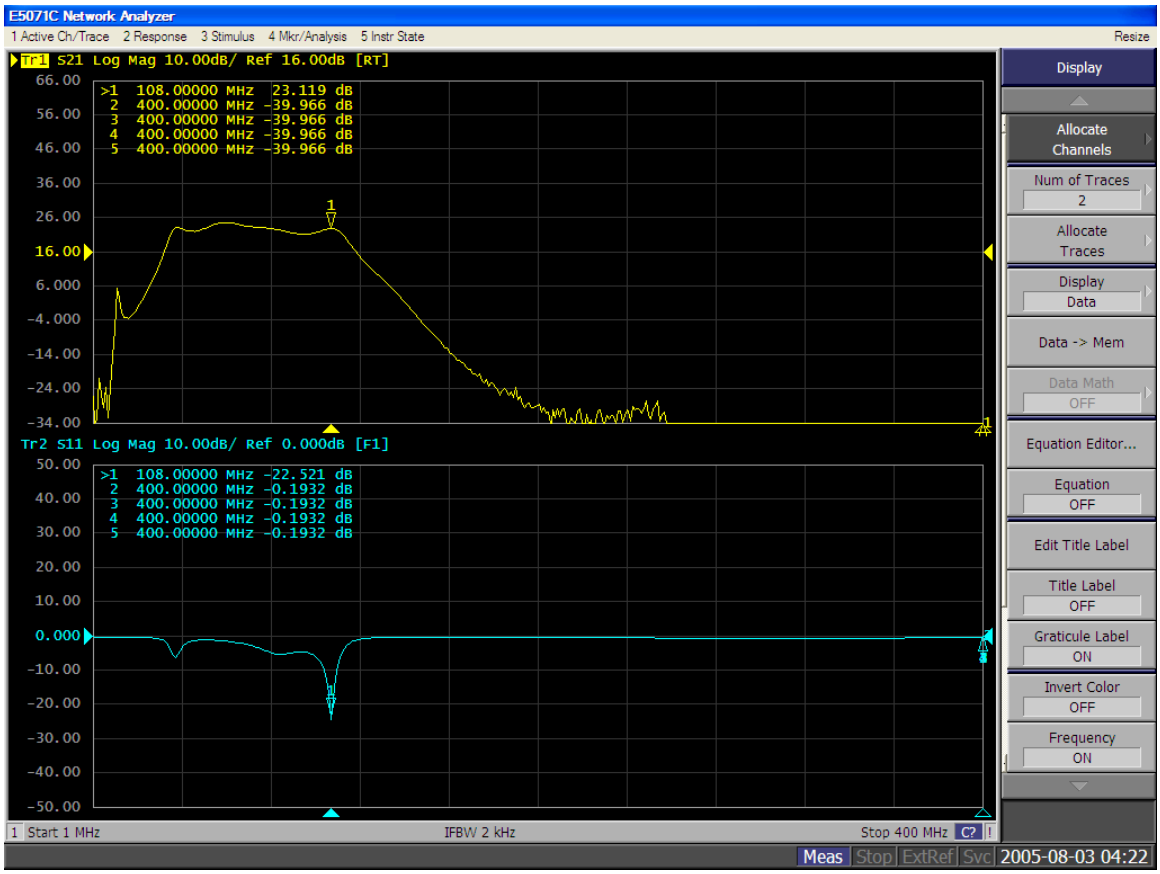


Table 5. Test Circuit Component Designations and Values

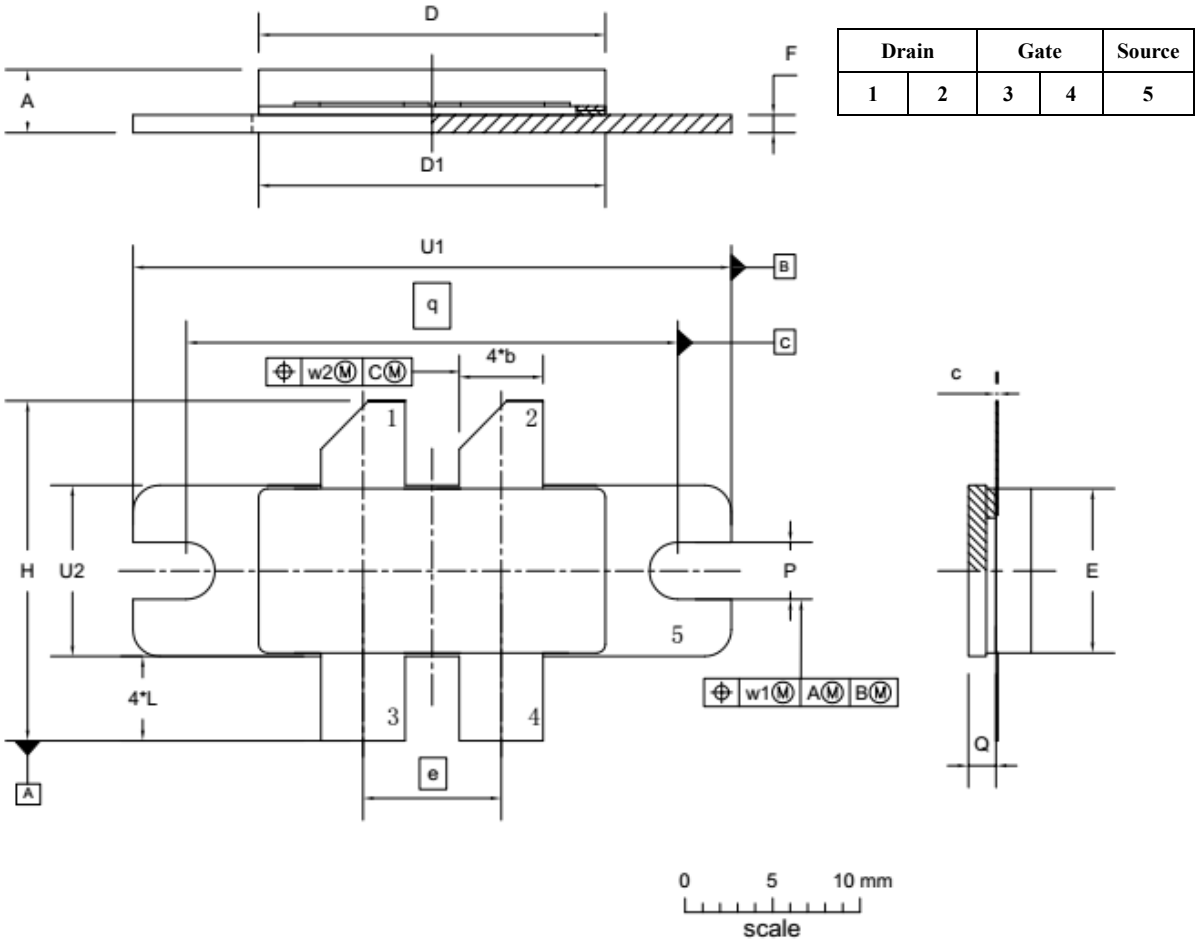
Component	Description	Suggested Manufacturer
C1~C2,	360pF MQ301111	
R1,R2	360Ω 0805	
C3	100pF MQ301111	
C8,C10,C12,C13,C16,C17	10uF 1210	
C4,C7	200pF MQ301111	
C5	150pF MQ301111	
C6	150pF MQ301111	
C9,C11,C14,C15,C22,C23	1000pF MQ301111	
C18	15pF MQ301111	
C19	47pF / MQ101111	
C20	62pF / MQ101111	
L1	2.5mm wire ， 8mm inner diameter, 2Turns	DIY
L1,L2	0.8mm wire ， 3mm inner diameter, 1.4Turns	DIY
L3,L4	0.8mm wire ， 3mm inner diameter, 2Turns	DIY
L5,L6	2mm wire ， 5mm inner diameter, 6Turns	DIY
L7,L8	2mm wire ， 5mm inner diameter, 2Turns	DIY

Figure 2： Network analyzer output S21/S11



Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.93 4.67	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/6/15	Rev 1.0	Advanced Datasheet

Application data based on SYX-26-32

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